



Q77H2-AD

Rev : A

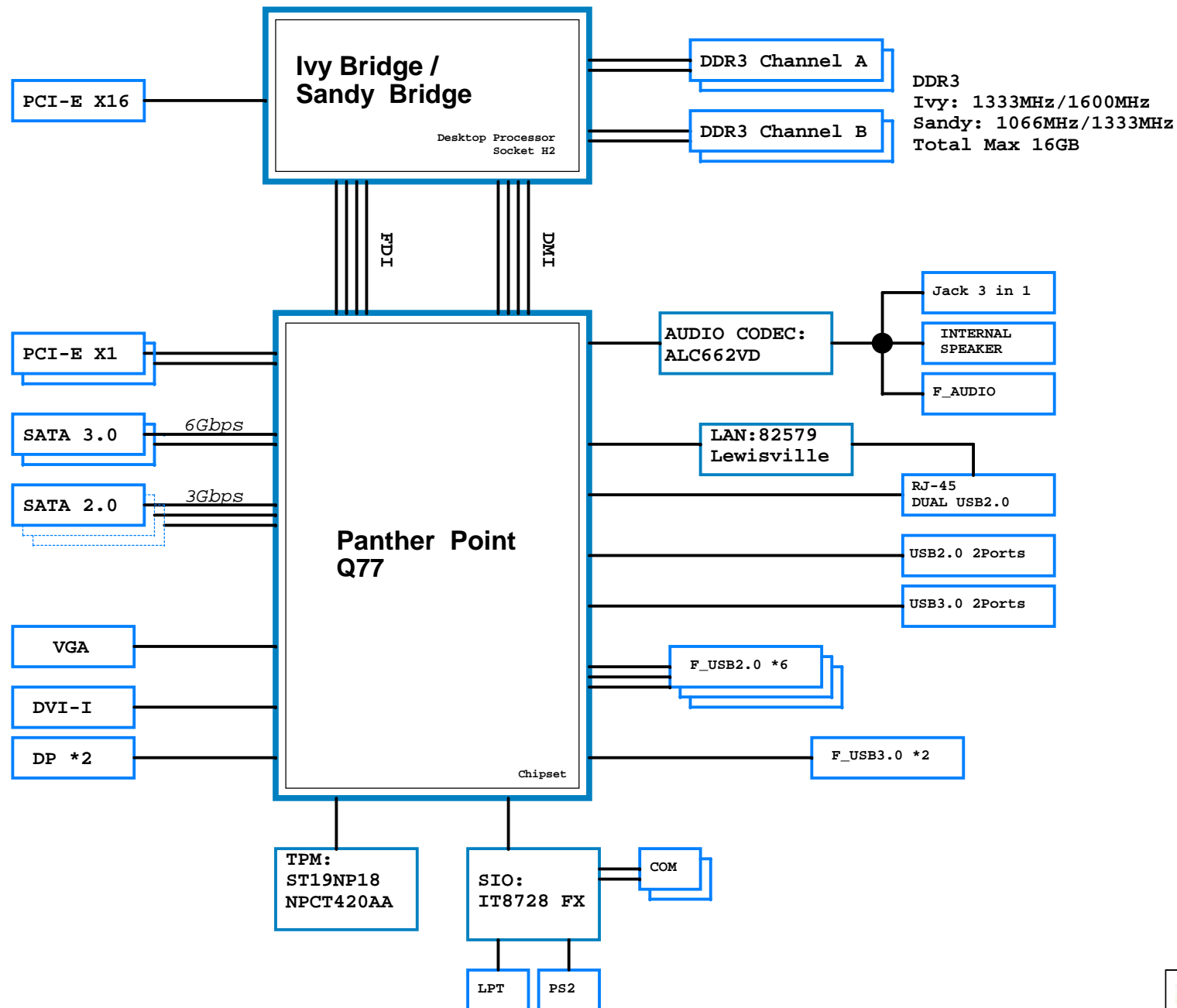
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22	LAN PHY - 82579, USBLAN
23	LAN (BCM5761) MAIN LINK
24	LAN (BCM5761) XTAL,GPIO
25	LAN (BCM5761) PWR & GND

NOTE:

REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version
26	AUDIO ALC662-VD	
27	Audio Connector(PANEL)	
28	USB2.0 CONNECTOR	
29	USB3.0 CONNECTOR	
30	DISPLAY PORT1	
31	DISPLAY PORT2	
32	DVI-I CONNECTOR	
33	VGA SCH	
34	SIO IT8728F	
35	TPM, PS/2, LPT	
36	FAN, COM	
37	F_PANEL, BUZ	
38	SEQUENCE CKT	
39	DC/DC 3VSB/3VDUAL/5VDUAL	
40	DC/DC VDIMM/DDR_VTT	
41	DC/DC CPU_VTT	
42	DC/DC V1P05_PCH,ME/V1P8_SFR	
43	DC/DC VCCSA, ATXPWR	
44	DC/DC VCORE/VAXG1	
45	DC/DC VCORE/VAXG2	
46	XDP	
47	Power Delivery	
48	PWR Sequence, RST Diagram	
49	Clock Distribution	



GPIO Table

PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4SS

IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

Strapping Table

PCH Strapping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

SIO IT8728F D/EX Strapping (Page.28)

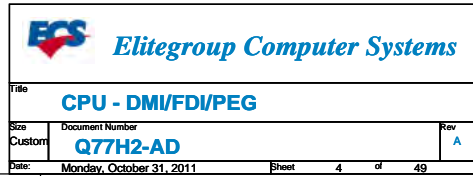
Power-On Strapping

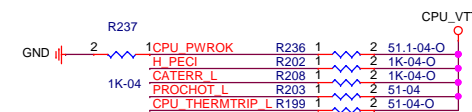
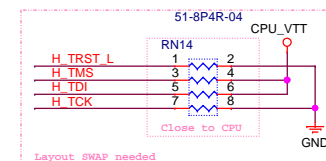
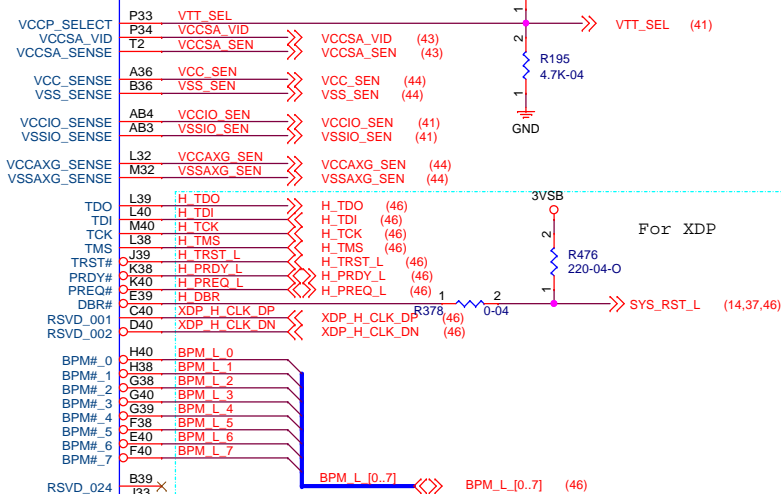
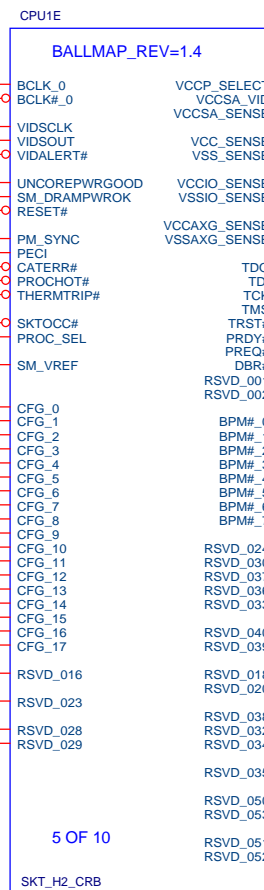
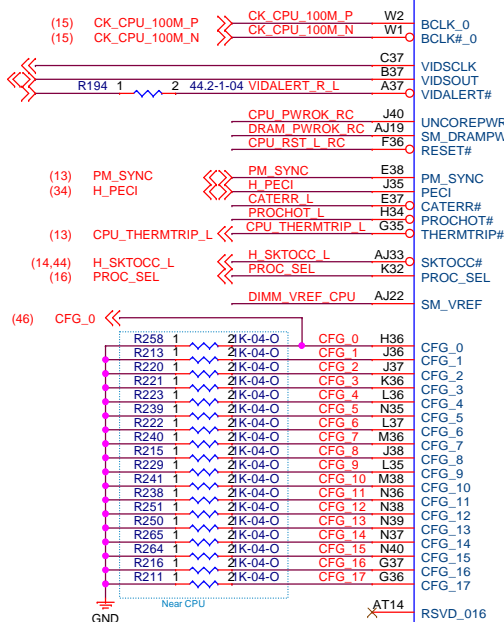
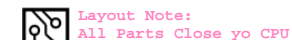
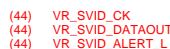
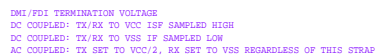
	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-48		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-29	OV/UV	0	Force Mode



Elitegroup Computer Systems

Title			GPIO Function Map		
Size	Document Number				Rev
Custom	Q77H2-AD				A
Date:	Monday, October 31, 2011		Sheet	3	of 49





CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSA[0]_X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	+	+	PEOFGSEL[0]
6	+	+	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

(9) M_DATA_A[0..63]	← M_DATA A[0..63]
(9) M_DQS_A_P[0..7]	← M_DQS A P[0..7]
(9) M_DQS_A_N[0..7]	← M_DQS A N[0..7]
(9) M_MA_A[0..15]	← M_MA A[0..15]
(9) M_BS_A[0..2]	← M_BS A[0..2]
(9) M_CS_A_L[0..3]	← M_CS A L[0..3]
(9) M_CKE_A[0..3]	← M_CKE A[0..3]
(9) M_ODT_A[0..3]	← M_ODT A[0..3]
(9) M_CLK_A_P[0..3]	← M_CLK A P[0..3]
(9) M_CLK_A_N[0..3]	← M_CLK A N[0..3]
(9) M_WE_A_L	← M_WE A L
(9) M_CAS_A_L	← M_CAS A L
(9) M_RAS_A_L	← M_RAS A L

DDR3 CH.A

(10,9) DDR3_DRAMRST_L ← DDR3_DRAMRST_L

(10) M_DATA_B[0..63]	← M_DATA B[0..63]
(10) M_DQS_B_P[0..7]	← M_DQS B P[0..7]
(10) M_DQS_B_N[0..7]	← M_DQS B N[0..7]
(10) M_MA_B[0..15]	← M_MA B[0..15]
(10) M_BS_B[0..2]	← M_BS B[0..2]
(10) M_CS_B_L[0..3]	← M_CS B L[0..3]
(10) M_CKE_B[0..3]	← M_CKE B[0..3]
(10) M_ODT_B[0..3]	← M_ODT B[0..3]
(10) M_CLK_B_P[0..3]	← M_CLK B P[0..3]
(10) M_CLK_B_N[0..3]	← M_CLK B N[0..3]
(10) M_WE_B_L	← M_WE B L
(10) M_CAS_B_L	← M_CAS B L
(10) M_RAS_B_L	← M_RAS B L

DDR3 CH.B

CPU1C			
BALLMAP_REV=1.4			
M_DATA A0	AJ3	SA_DQ_0	
M_DATA A1	AJ4	SA_DQ_1	
M_DATA A2	AL3	SA_DQ_2	
M_DATA A3	AL4	SA_DQ_3	
M_DATA A4	AJ2	SA_MA_4	
M_DATA A5	AJ1	SA_DQ_5	
M_DATA A6	AL2	SA_DQ_6	
M_DATA A7	AL1	SA_DQ_7	
M_DATA A8	AN1	SA_DQ_8	
M_DATA A9	AN4	SA_DQ_9	
M_DATA A10	AR3	SA_MA_10	
M_DATA A11	AR4	SA_DQ_11	
M_DATA A12	AN2	SA_DQ_12	
M_DATA A13	AN3	SA_DQ_13	
M_DATA A14	AR2	SA_DQ_14	
M_DATA A15	AR1	SA_DQ_15	
M_DATA A16	AV2	SA_DQ_16	
M_DATA A17	AW3	SA_DQ_17	
M_DATA A18	AV5	SA_DQ_18	
M_DATA A19	AW5	SA_DQ_19	
M_DATA A20	AU2	SA_DQ_20	
M_DATA A21	AU3	SA_DQ_21	
M_DATA A22	AU5	SA_DQ_22	
M_DATA A23	AV6	SA_DQ_23	
M_DATA A24	AV7	SA_DQ_24	
M_DATA A25	AU7	SA_DQ_25	
M_DATA A26	AV9	SA_DQ_26	
M_DATA A27	AU9	SA_DQ_27	
M_DATA A28	AV7	SA_DQ_28	
M_DATA A29	AW7	SA_DQ_29	
M_DATA A30	AW9	SA_DQ_30	
M_DATA A31	AY9	SA_DQ_31	
M_DATA A32	AU35	SA_DQ_32	
M_DATA A33	AW37	SA_DQ_33	
M_DATA A34	AU39	SA_DQ_34	
M_DATA A35	AU36	SA_DQ_35	
M_DATA A36	AW35	SA_DQ_36	
M_DATA A37	AY36	SA_DQ_37	
M_DATA A38	AU38	SA_DQ_38	
M_DATA A39	AU37	SA_DQ_39	
M_DATA A40	AR40	SA_DQ_40	
M_DATA A41	AR37	SA_DQ_41	
M_DATA A42	AN38	SA_DQ_42	
M_DATA A43	AN37	SA_DQ_43	
M_DATA A44	AR39	SA_DQ_44	
M_DATA A45	AR38	SA_DQ_45	
M_DATA A46	AN39	SA_DQ_46	
M_DATA A47	AN40	SA_DQ_47	
M_DATA A48	AL40	SA_DQ_48	
M_DATA A49	AL37	SA_DQ_49	
M_DATA A50	AJ38	SA_DQ_50	
M_DATA A51	AJ37	SA_DQ_51	
M_DATA A52	AL39	SA_DQ_52	
M_DATA A53	AL38	SA_DQ_53	
M_DATA A54	AJ39	SA_DQ_54	
M_DATA A55	AJ40	SA_DQ_55	
M_DATA A56	AG40	SA_DQ_56	
M_DATA A57	AG37	SA_DQ_57	
M_DATA A58	AE38	SA_DQ_58	
M_DATA A59	AE37	SA_DQ_59	
M_DATA A60	AG39	SA_DQ_60	
M_DATA A61	AG38	SA_DQ_61	
M_DATA A62	AE39	SA_DQ_62	
M_DATA A63	AE40	SA_DQ_63	
M_DQS A P0	AK3	SA_DQS_0	
M_DQS A P1	AP3	SA_DQS_1	
M_DQS A P2	AW4	SA_DQS_2	
M_DQS A P3	AV8	SA_DQS_3	
M_DQS A P4	AV37	SA_DQS_4	
M_DQS A P5	AP38	SA_DQS_5	
M_DQS A P6	AK38	SA_DQS_6	
M_DQS A P7	AF38	SA_DQS_7	
M_DQS A N0	AK2	SA_DQS#_0	
M_DQS A N1	AP2	SA_DQS#_1	
M_DQS A N2	AV4	SA_DQS#_2	
M_DQS A N3	AW8	SA_DQS#_3	
M_DQS A N4	AV36	SA_DQS#_4	
M_DQS A N5	AP39	SA_DQS#_5	
M_DQS A N6	AK39	SA_DQS#_6	
M_DQS A N7	AF39	SA_DQS#_7	

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
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SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0

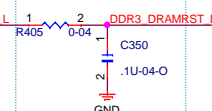
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SKT_H2_CRB

DDR3 CH.A

AV27	M_MA A0
AV24	M_MA A1
AW24	M_MA A2
AW23	M_MA A3
AV23	M_MA A4
AT24	M_MA A5
AV23A	M_MA A6
AV22	M_MA A7
AV22	M_MA A8
AT22	M_MA A9
AV28	M_MA A10
AU21	M_MA A11
AT21	M_MA A12
AW32	M_MA A13
AU20	M_MA A14
AT20	M_MA A15
AW29	M_WE A L
AV30	M_CAS A L
AU28	M_RAS A L
AV29	M_BS A0
AW28	M_BS A1
AV20	M_BS A2
AU29	M_CS A L0
AW29	M_CS A L1
AW30	M_CS A L2
AU33	M_CS A L3
AV19	M_CKE A0
AT19	M_CKE A1
AU18	M_CKE A2
AV18	M_CKE A3
AV31	M_ODT A0
AU32	M_ODT A1
AU30	M_ODT A2
AW33	M_ODT A3
AY25	M_CLK A P0
AW25	M_CLK A N0
AU24	M_CLK A P1
AU25	M_CLK A N1
AW27	M_CLK A P2
AY27	M_CLK A N2
AV26	M_CLK A P3
AW26	M_CLK A N3
AW18	DDR3_DRAMRST_R L
AV13	
AV12	
AU12	
AU14	
AW13	
AY13	
AU15	
AU11	
AY12	
AW12	

Desktop doesn't support ecc



For RC Filter

Pay Attention to This Part!

M_DATA B0	AG7
M_DATA B1	AG8
M_DATA B2	AJ9
M_DATA B3	AJ8
M_DATA B4	AG5
M_DATA B5	AG6
M_DATA B6	AJ6
M_DATA B7	AJ7
M_DATA B13	AL7
M_DATA B11	AM7
M_DATA B11	AM10
M_DATA B15	AL10
M_DATA B12	AL6
M_DATA B8	AM6
M_DATA B14	AL9
M_DATA B10	AM9
M_DATA B16	AP7
M_DATA B17	AR7
M_DATA B18	AP10
M_DATA B19	AR10
M_DATA B20	AP6
M_DATA B21	AR6
M_DATA B22	AP9
M_DATA B23	AR9
M_DATA B24	AM12
M_DATA B25	AM13
M_DATA B26	AR13
M_DATA B27	AP13
M_DATA B28	AL12
M_DATA B29	AP12
M_DATA B30	AR12
M_DATA B31	AP12
M_DATA B32	AR28
M_DATA B33	AR29
M_DATA B34	AL28
M_DATA B35	AL29
M_DATA B36	AP28
M_DATA B37	AP29
M_DATA B38	AM28
M_DATA B39	AM29
M_DATA B40	AP32
M_DATA B41	AP31
M_DATA B42	AP35
M_DATA B43	AP34
M_DATA B44	AR32
M_DATA B45	AR31
M_DATA B46	AR32
M_DATA B47	AR34
M_DATA B48	AM32
M_DATA B52	AM31
M_DATA B55	AL35
M_DATA B51	AL32
M_DATA B54	AM34
M_DATA B49	AL31
M_DATA B53	AM35
M_DATA B50	AL34
M_DATA B56	AH35
M_DATA B57	AH34
M_DATA B58	AE34
M_DATA B59	AE35
M_DATA B60	AJ35
M_DATA B61	AJ34
M_DATA B62	AF33
M_DATA B63	AF35

M_DQS B P0	AH7
M_DQS B P1	AM8
M_DQS B P2	AR8
M_DQS B P3	AN13
M_DQS B P4	AN29
M_DQS B P5	AP33
M_DQS B P6	AL33
M_DQS B P7	AG35

M_DQS B N0	AH6
M_DQS B N1	AL8
M_DQS B N2	AP8
M_DQS B N3	AN12
M_DQS B N4	AN28
M_DQS B N5	AR33
M_DQS B N6	AM33
M_DQS B N7	AG34

CPU1D

BALLMAP_REV=1.4			
SB_DQ_0		SB_MA_0	
SB_DQ_1		SB_MA_1	
SB_DQ_2		SB_MA_2	
SB_DQ_3		SB_MA_3	
SB_DQ_4		SB_MA_4	
SB_DQ_5		SB_MA_5	
SB_DQ_6		SB_MA_6	
SB_DQ_7		SB_MA_7	
SB_DQ_8		SB_MA_8	
SB_DQ_9		SB_MA_9	
SB_DQ_10		SB_MA_10	
SB_DQ_11		SB_MA_11	
SB_DQ_12		SB_MA_12	
SB_DQ_13		SB_MA_13	
SB_DQ_14		SB_MA_14	
SB_DQ_15		SB_MA_15	
SB_DQ_16			
SB_DQ_17		SA_CK[2]	
SB_DQ_18		SA_CK[1]	
SB_DQ_19		SA_ODT[2]	
SB_DQ_20			
SB_DQ_21			
SB_DQ_22			
SB_DQ_23		SB_BS_0	
SB_DQ_24		SB_BS_1	
SB_DQ_25		SB_BS_2	
SB_DQ_26			
SB_DQ_27			
SB_DQ_28		SB_CS#_0	
SB_DQ_29		SB_CS#_1	
SB_DQ_30		SB_CS#_2	
SB_DQ_31		SB_CS#_3	
SB_DQ_32			
SB_DQ_33			
SB_DQ_34			
SB_DQ_35		SB_CKE_0	
SB_DQ_36		SB_CKE_1	
SB_DQ_37		SB_CKE_2	
SB_DQ_38		SB_CKE_3	
SB_DQ_39			
SB_DQ_40			
SB_DQ_41			
SB_DQ_42		SB_ODT_0	
SB_DQ_43		SB_ODT_1	
SB_DQ_44		SB_ODT_2	
SB_DQ_45		SB_ODT_3	
SB_DQ_46			
SB_DQ_47			
SB_DQ_48			
SB_DQ_49		SB_CK_0	
SB_DQ_50		SB_CK#_0	
SB_DQ_51		SB_CK_1	
SB_DQ_52		SB_CK#_1	
SB_DQ_53		SB_CK_2	
SB_DQ_54		SB_CK#_2	
SB_DQ_55		SB_CK_3	
SB_DQ_56		SB_CK#_3	
SB_DQ_57			
SB_DQ_58			
SB_DQ_59			
SB_DQ_60			
SB_DQ_61			
SB_DQ_62			
SB_DQ_63			
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SB_DQS_2			
SB_DQS_3			
SB_DQS_4		SB_ECC_CB_0	
SB_DQS_5		SB_ECC_CB_1	
SB_DQS_6		SB_ECC_CB_2	
SB_DQS_7		SB_ECC_CB_3	
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DDR3 CH.B

DDR_1

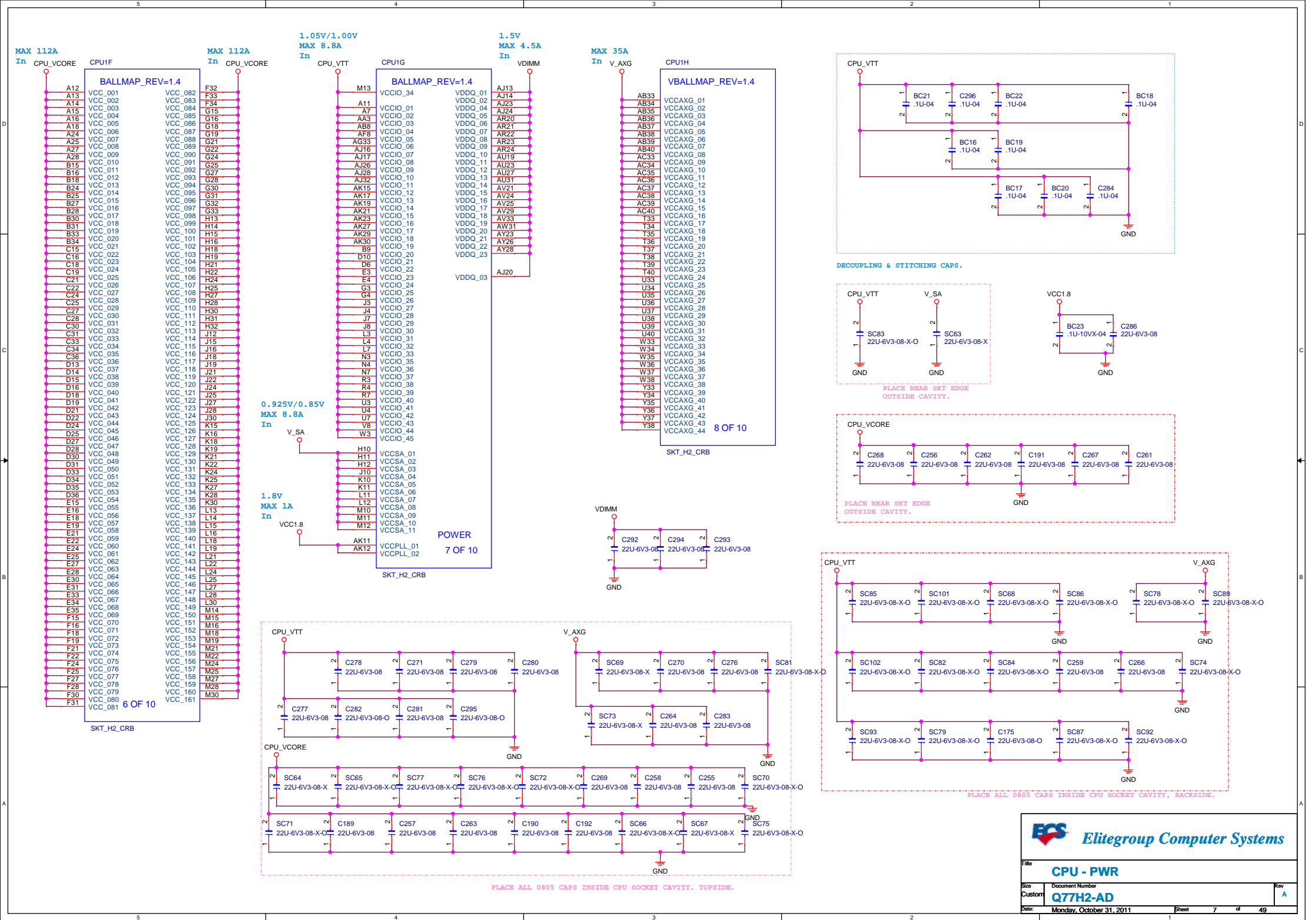
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SKT_H2_CRB

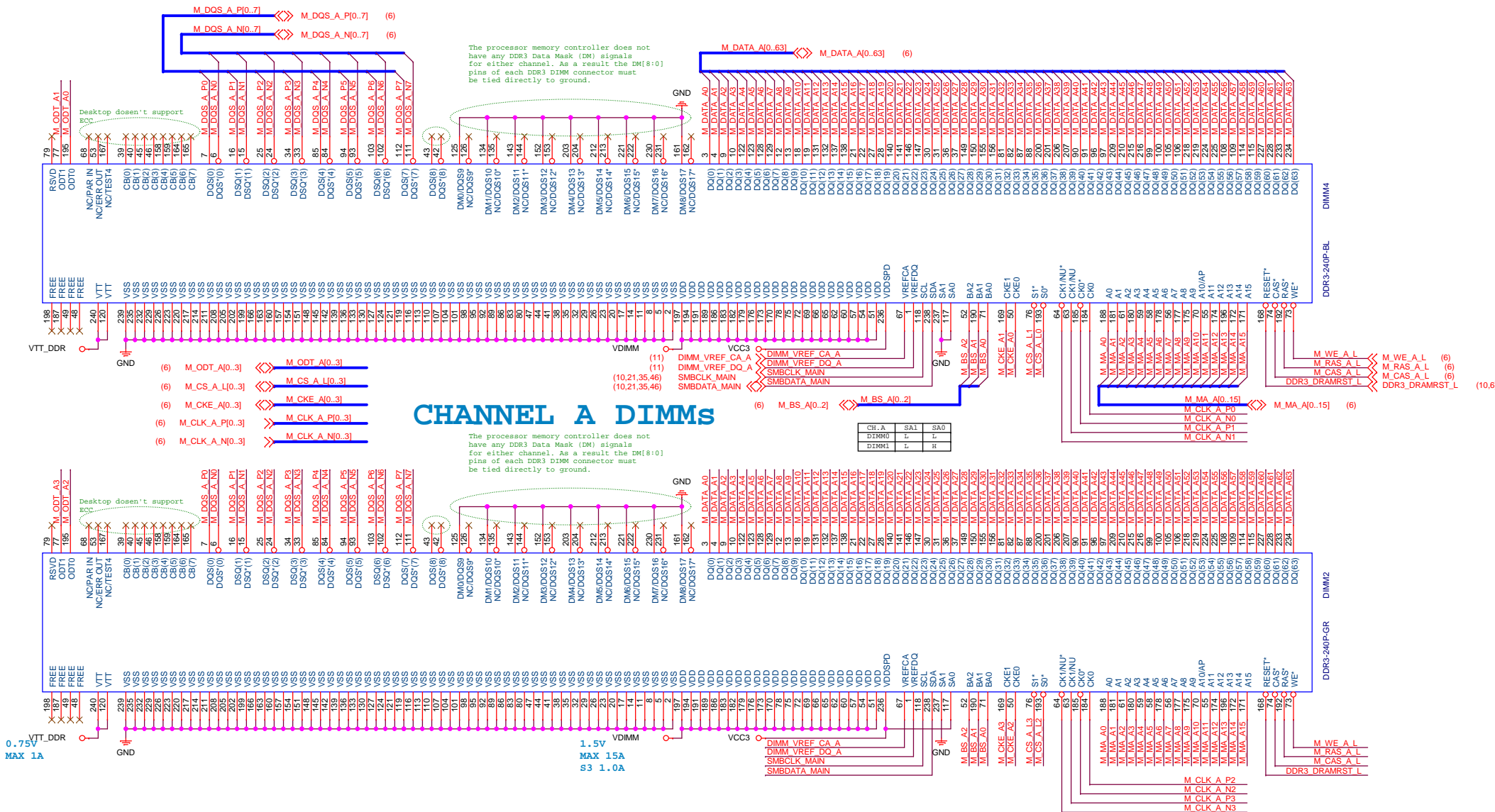
CPU - DDR3
Q77H2-AD

Title: CPU - DDR3
 Size: Q77H2-AD
 Custom: Q77H2-AD
 Date: Monday, October 31, 2011
 Sheet: 6 of 49

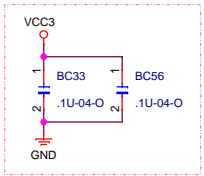
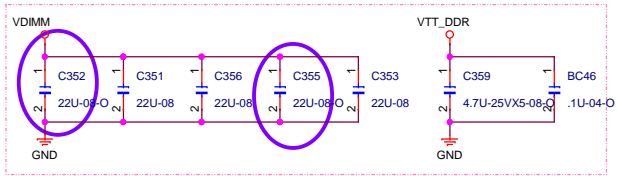
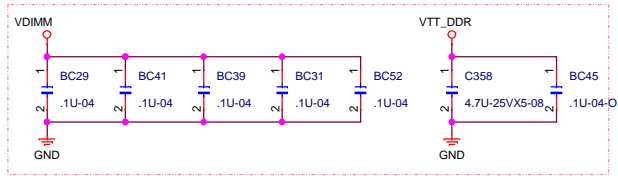
Rev: A

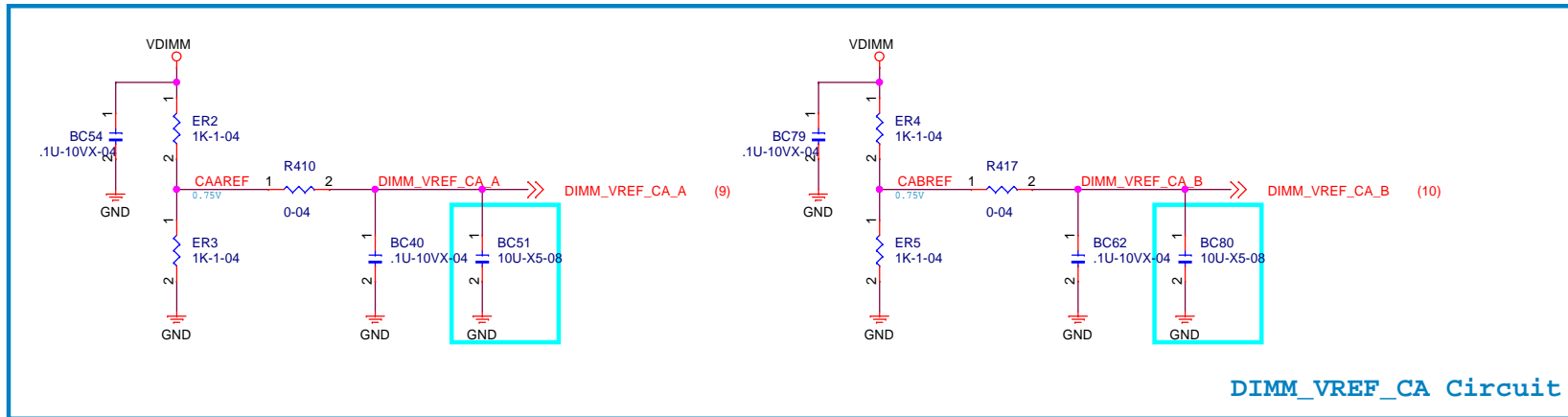
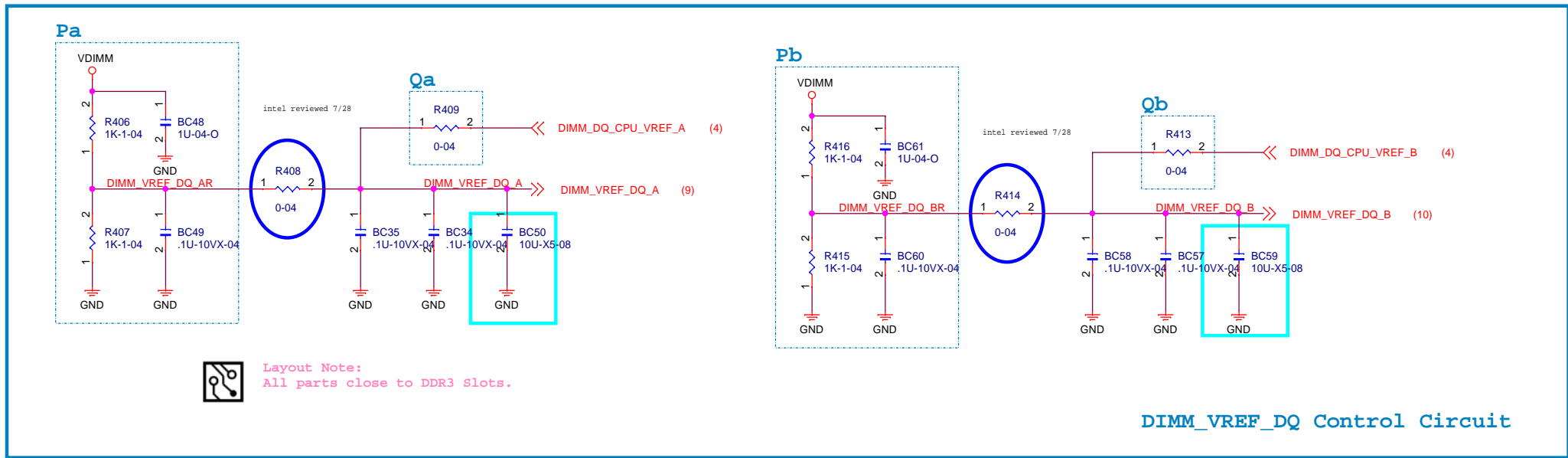


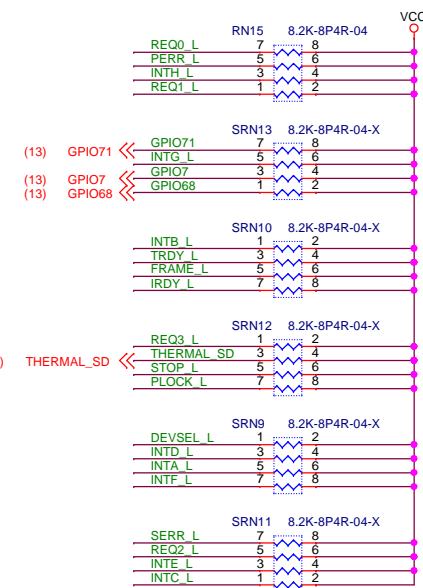
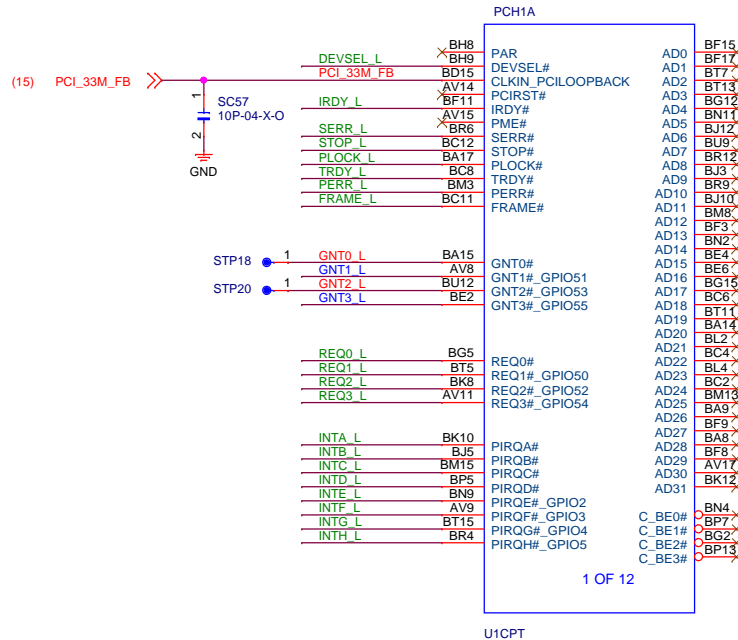
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A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM30	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM36	AV3	VSS_184	VSS_274	H2
A35	VSS_005	VSS_095	AM37	AV35	VSS_185	VSS_275	H20
AA33	VSS_006	VSS_096	AM38	AV38	VSS_186	VSS_276	H23
AA34	VSS_007	VSS_097	AM39	AV6	VSS_187	VSS_277	H26
AA35	VSS_008	VSS_098	AM40	AW10	VSS_188	VSS_278	H29
AA36	VSS_009	VSS_099	AM5	AW11	VSS_189	VSS_279	H33
AA37	VSS_010	VSS_100	AN10	AW14	VSS_190	VSS_280	H37
AA38	VSS_011	VSS_101	AN11	AW36	VSS_191	VSS_281	H39
AA6	VSS_012	VSS_102	AN14	AW6	VSS_192	VSS_282	H5
AB5	VSS_013	VSS_103	AN17	AY11	VSS_193	VSS_283	H6
AC1	VSS_014	VSS_104	AN19	AY14	VSS_194	VSS_284	H9
AC6	VSS_015	VSS_105	AN22	AY18	VSS_195	VSS_285	H9
AD33	VSS_016	VSS_106	AN24	AY35	VSS_196	VSS_286	J11
AD38	VSS_017	VSS_107	AN27	AY37	VSS_197	VSS_287	J20
AD39	VSS_018	VSS_108	AN30	AY6	VSS_198	VSS_288	J23
AD40	VSS_019	VSS_109	AN31	AY8	VSS_199	VSS_289	J26
AD5	VSS_020	VSS_110	AN32	B10	VSS_200	VSS_290	J29
AD8	VSS_021	VSS_111	AN33	B13	VSS_201	VSS_291	J32
AE3	VSS_022	VSS_112	AN34	B14	VSS_202	VSS_292	J32
AE33	VSS_023	VSS_113	AN35	B17	VSS_203	VSS_293	K1
AE36	VSS_024	VSS_114	AN36	B23	VSS_204	VSS_294	K12
AF1	VSS_025	VSS_115	AN5	B29	VSS_205	VSS_295	K13
AF34	VSS_026	VSS_116	AN6	B26	VSS_206	VSS_296	K14
AF36	VSS_027	VSS_117	AN7	B25	VSS_207	VSS_297	K17
AF37	VSS_028	VSS_118	AN8	B32	VSS_208	VSS_298	K2
AF40	VSS_029	VSS_119	AN9	B38	VSS_209	VSS_299	K23
AF5	VSS_030	VSS_120	AP1	B6	VSS_210	VSS_300	K26
AF6	VSS_031	VSS_121	AP11	C11	VSS_211	VSS_301	K29
AF7	VSS_032	VSS_122	AP14	C12	VSS_212	VSS_302	K29
AC36	VSS_033	VSS_123	AP17	C17	VSS_213	VSS_303	K35
AH2	VSS_034	VSS_124	AP22	C20	VSS_214	VSS_304	K37
AH3	VSS_035	VSS_125	AP25	C23	VSS_215	VSS_305	K39
AH33	VSS_036	VSS_126	AP27	C26	VSS_216	VSS_306	K5
AH36	VSS_037	VSS_127	AP30	C29	VSS_217	VSS_307	K6
AH37	VSS_038	VSS_128	AP36	C32	VSS_218	VSS_308	K6
AH38	VSS_039	VSS_129	AP37	C35	VSS_219	VSS_309	L10
AH39	VSS_040	VSS_130	AP4	C7	VSS_220	VSS_310	L17
AH40	VSS_041	VSS_131	AP40	C8	VSS_221	VSS_311	L20
AH5	VSS_042	VSS_132	AP5	D17	VSS_222	VSS_312	L23
AH8	VSS_043	VSS_133	AR11	D2	VSS_223	VSS_313	L26
AJ12	VSS_044	VSS_134	AR14	D20	VSS_224	VSS_314	L29
AJ15	VSS_045	VSS_135	AR15	D23	VSS_225	VSS_315	L8
AJ18	VSS_046	VSS_136	AR18	D26	VSS_226	VSS_316	M1
AJ21	VSS_047	VSS_137	AR19	D29	VSS_227	VSS_317	M17
AJ25	VSS_048	VSS_138	AR27	D32	VSS_228	VSS_318	M2
AJ27	VSS_049	VSS_139	AR30	D37	VSS_229	VSS_319	M20
AJ36	VSS_050	VSS_140	AR36	D39	VSS_230	VSS_320	M23
AJ5	VSS_051	VSS_141	AR5	D4	VSS_231	VSS_321	M26
AK1	VSS_052	VSS_142	AT1	D5	VSS_232	VSS_322	M29
AK10	VSS_053	VSS_143	AT10	D5	VSS_233	VSS_323	M33
AK13	VSS_054	VSS_144	AT12	D5	VSS_234	VSS_324	M35
AK14	VSS_055	VSS_145	AT13	E12	VSS_235	VSS_325	M37
AK16	VSS_056	VSS_146	AT15	E17	VSS_236	VSS_326	M39
AK22	VSS_057	VSS_147	AT16	E20	VSS_237	VSS_327	M5
AK28	VSS_058	VSS_148	AT17	E23	VSS_238	VSS_328	M6
AK31	VSS_059	VSS_149	AT12	E26	VSS_239	VSS_329	M9
AK32	VSS_060	VSS_150	AT25	E29	VSS_240	VSS_330	N8
AK33	VSS_061	VSS_151	AT27	E32	VSS_241	VSS_331	P1
AK34	VSS_062	VSS_152	AT28	E36	VSS_242	VSS_332	P2
AK35	VSS_063	VSS_153	AT29	E7	VSS_243	VSS_333	P36
AK36	VSS_064	VSS_154	AT3	E8	VSS_244	VSS_334	P38
AK37	VSS_065	VSS_155	AT30	F1	VSS_245	VSS_335	P40
AK4	VSS_066	VSS_156	AT31	F10	VSS_246	VSS_336	P5
AK40	VSS_067	VSS_157	AT32	F13	VSS_247	VSS_337	P6
AK5	VSS_068	VSS_158	AT33	F14	VSS_248	VSS_338	R33
AK6	VSS_069	VSS_159	AT34	F17	VSS_249	VSS_339	R35
AK7	VSS_070	VSS_160	AT35	F20	VSS_250	VSS_340	R37
AK8	VSS_071	VSS_161	AT36	F22	VSS_251	VSS_341	R8
AK9	VSS_072	VSS_162	AT37	F23	VSS_252	VSS_342	R9
AL11	VSS_073	VSS_163	AT38	F26	VSS_253	VSS_343	T1
AL14	VSS_074	VSS_164	AT39	F29	VSS_254	VSS_344	T5
AL17	VSS_075	VSS_165	AT4	F35	VSS_255	VSS_345	T6
AL19	VSS_076	VSS_166	AT40	F37	VSS_256	VSS_346	U1
AL24	VSS_077	VSS_167	AT5	F39	VSS_257	VSS_347	U8
AL27	VSS_078	VSS_168	AT6	F5	VSS_258	VSS_348	V3
AL30	VSS_079	VSS_169	AT7	F6	VSS_259	VSS_349	V34
AL36	VSS_080	VSS_170	AT8	F9	VSS_260	VSS_350	V35
AL5	VSS_081	VSS_171	AT9	G11	VSS_261	VSS_351	V36
AM1	VSS_082	VSS_172	AT9	G12	VSS_262	VSS_352	V37
AM11	VSS_083	VSS_173	AU1	G17	VSS_263	VSS_353	V38
AM14	VSS_084	VSS_174	AU26	G20	VSS_264	VSS_354	V39
AM17	VSS_085	VSS_175	AU34	G23	VSS_265	VSS_355	V40
AM2	VSS_086	VSS_176	AU4	G26	VSS_266	VSS_356	V5
AM21	VSS_087	VSS_177	AU6	G29	VSS_267	VSS_357	W6
AM23	VSS_088	VSS_178	AU8	G34	VSS_268	VSS_358	Y5
AM25	VSS_089	VSS_179	AV10	G7	VSS_269	VSS_359	Y8
	VSS_090	VSS_180			VSS_270	VSS_360	
A4	VSS_NCTF_01			AY37			
AV39	VSS_NCTF_02	9 OF 10		B3	VSS_NCTF_03	10 of 10	
					VSS_NCTF_04		
GND	SKT_H2_CRB		GND	GND	SKT_H2_CRB		



0.75V
MAX 1A



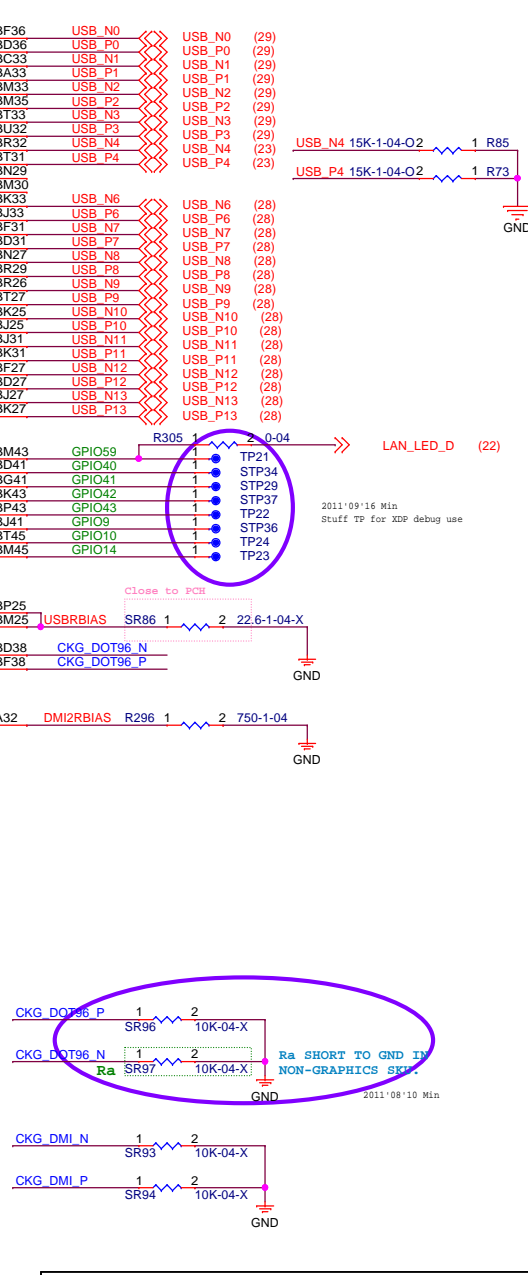
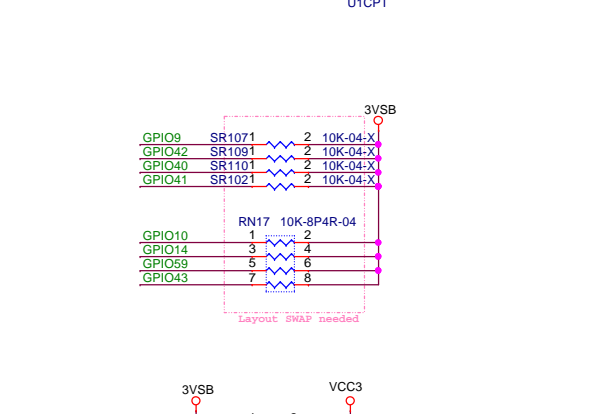
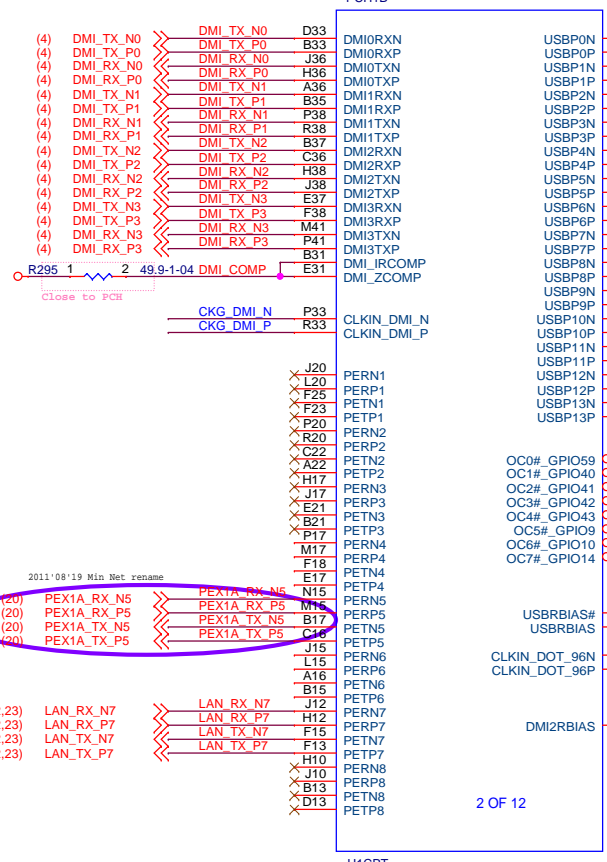




Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

* GNT1[0..3]# have been internal pull high to +VCC3



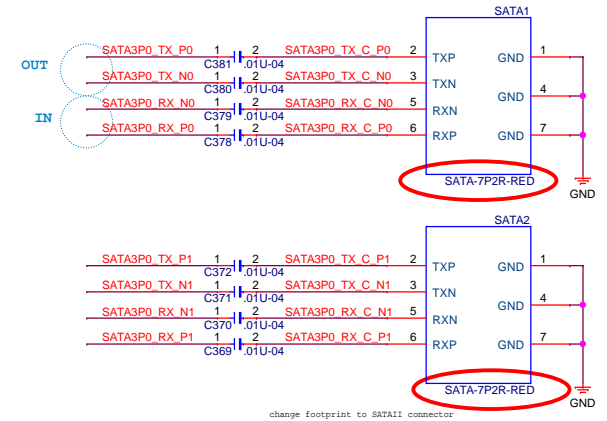
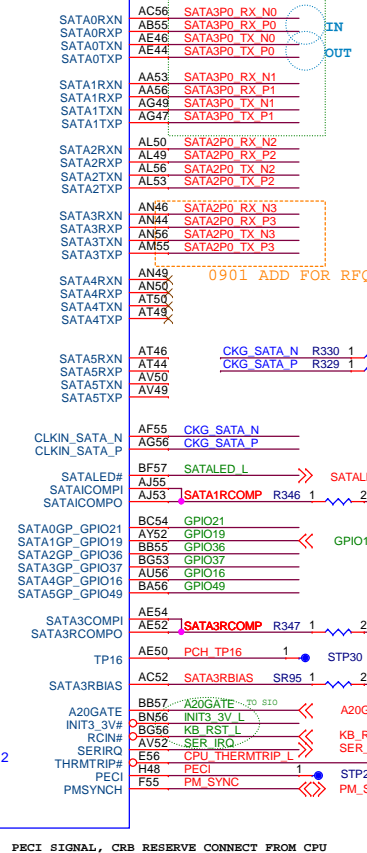
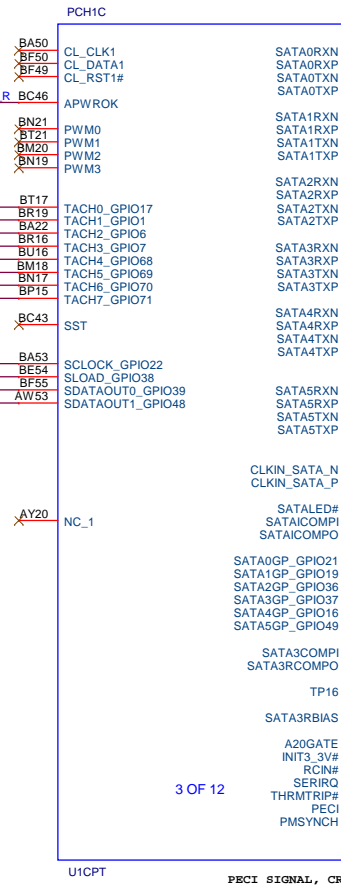
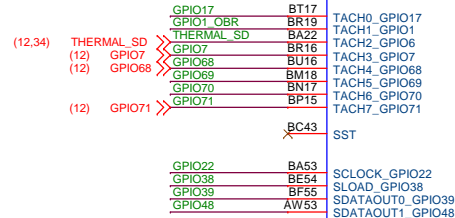
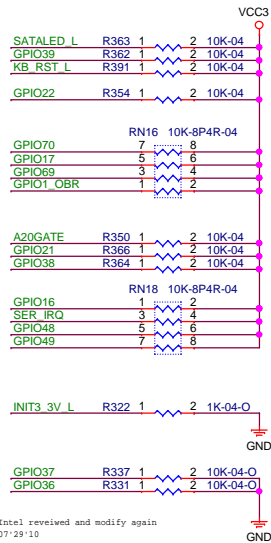
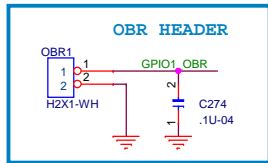
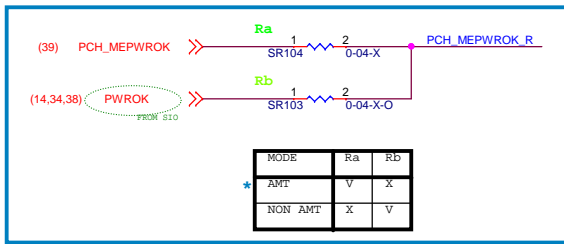
ECS Elitegroup Computer Systems

File: **PCH - DMI/PCI/PE/USB**

Size: Custom
Document Number: **Q77H2-AD**

Date: Monday, October 31, 2011
Sheet: 12 of 49

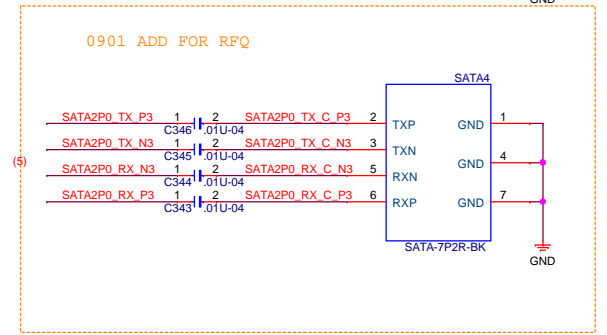
Rev: A



Layout Note:

SATA3.0 4.5/7.5/20 in 90 Q ±17.5%

SATA2.0 4.5/7.5/15 in 90 Q ±17.5%

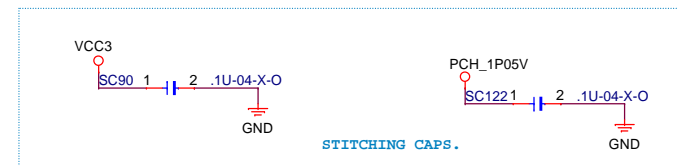
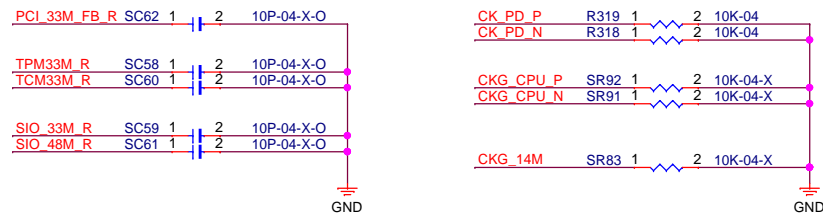
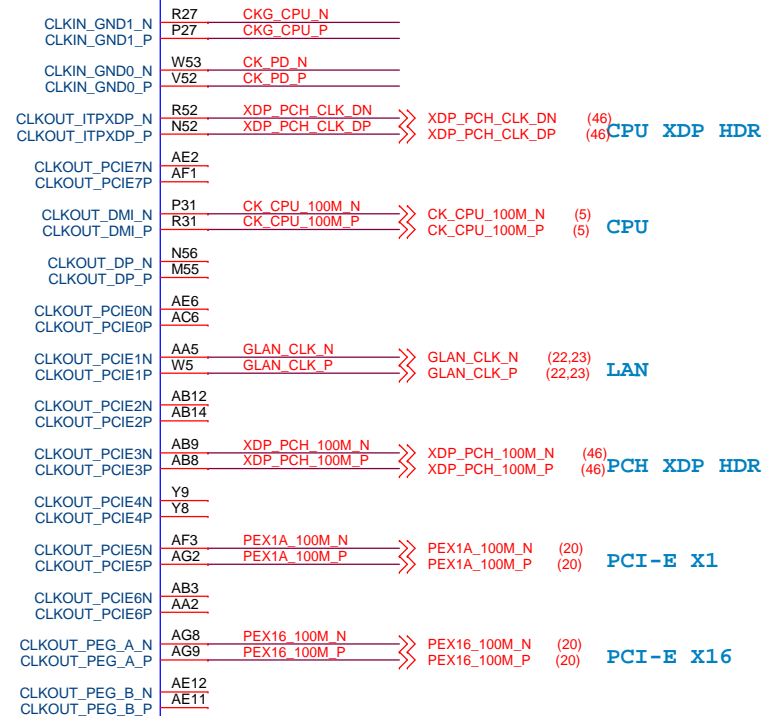
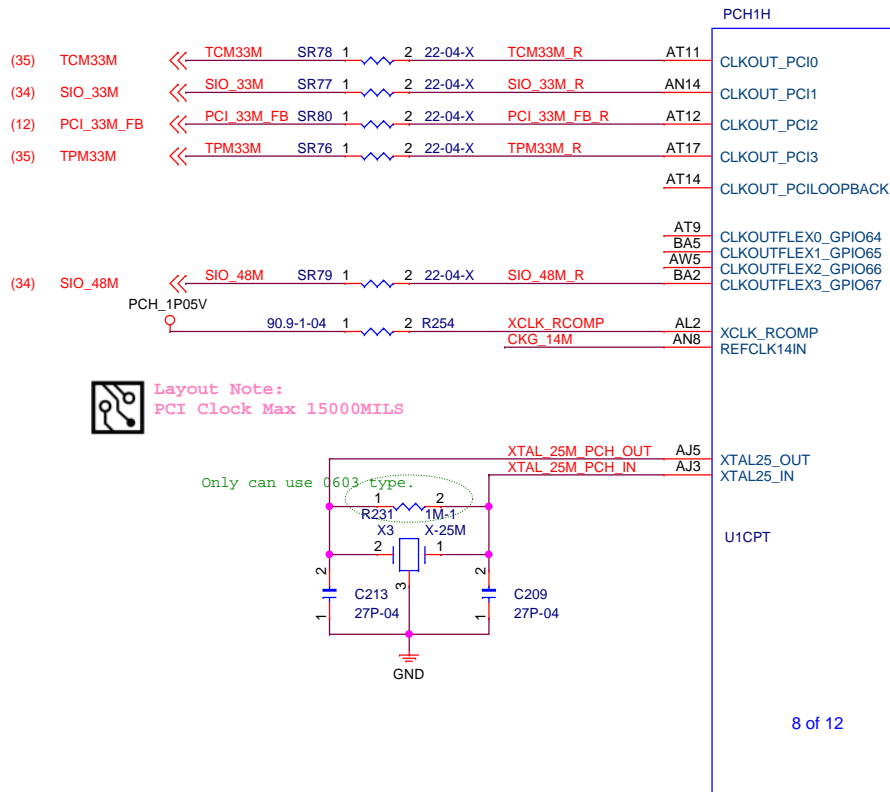


Elitegroup Computer Systems

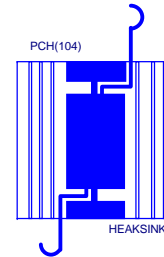
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Size: Custom Document Number: **Q77H2-AD** Rev: **A**

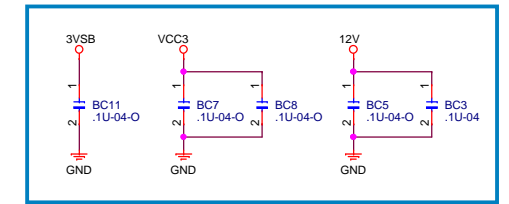
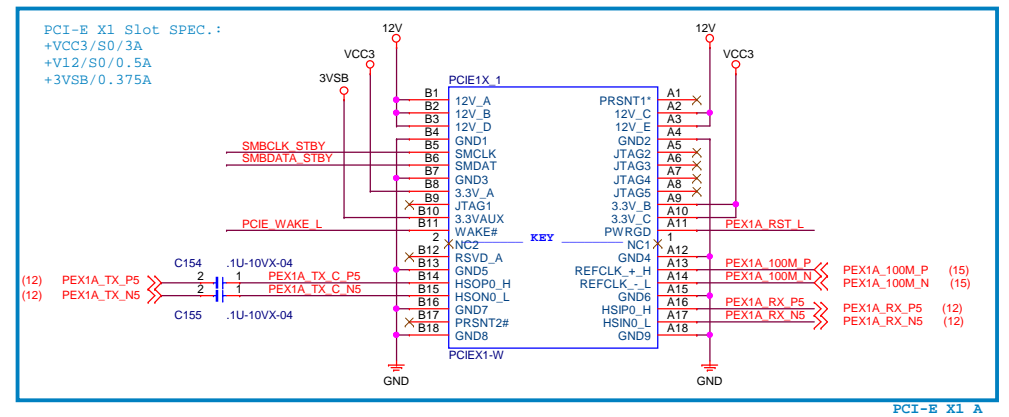
Date: **Monday, October 31, 2011** Sheet: **13** of **49**



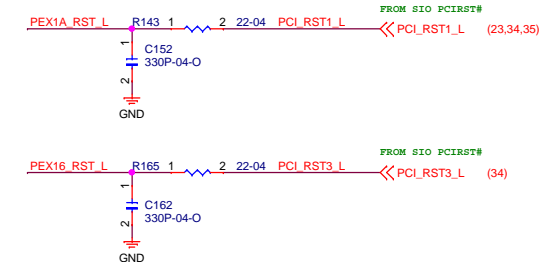




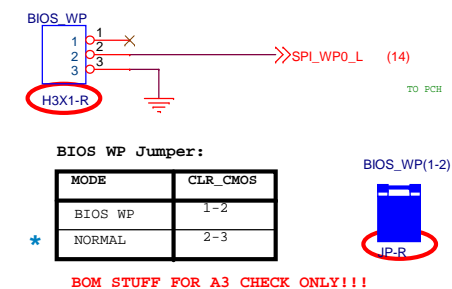
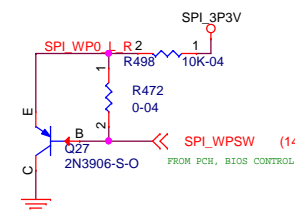
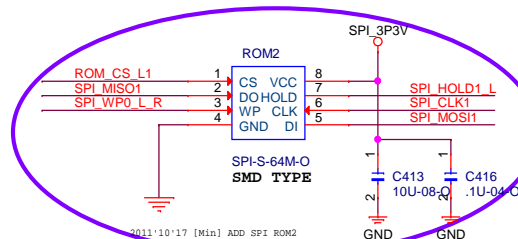
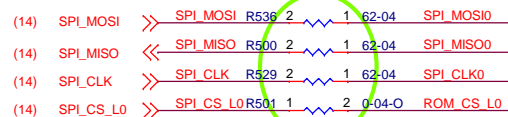
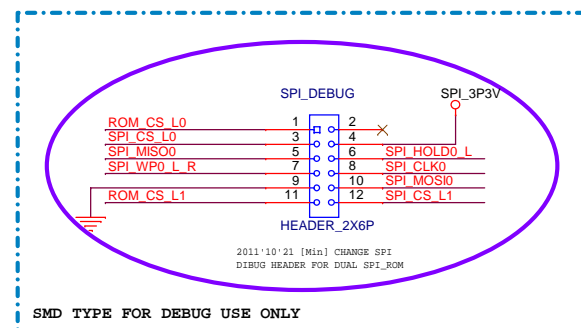
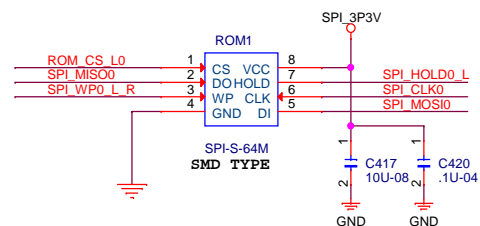
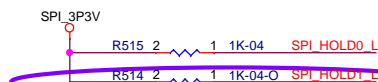
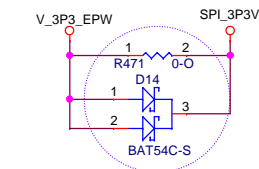
- +VCC3/S0/3A
- +V12/S0/5.5A
- +3VSB/0.375A



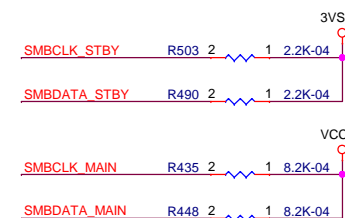
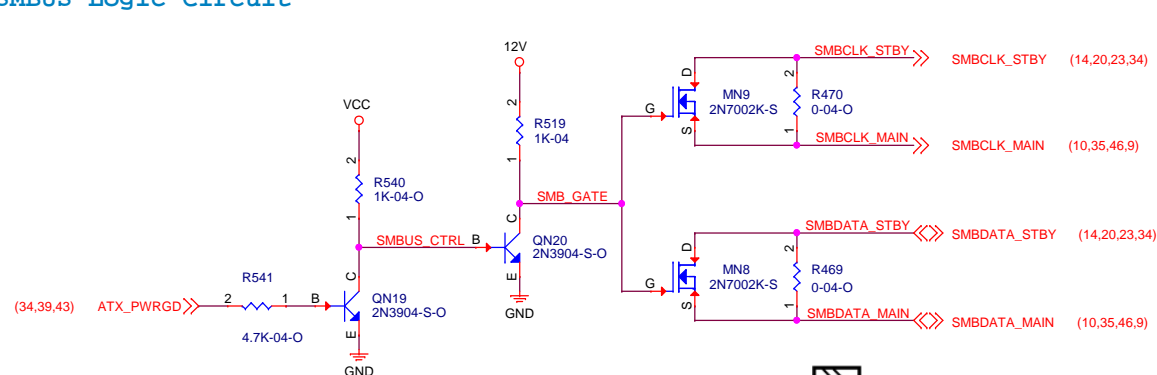
PCI-E X1 A Decoupling Cap.



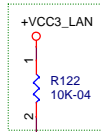
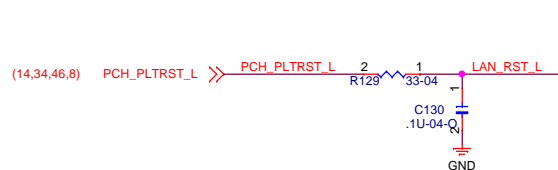
SPI ROM Circuit



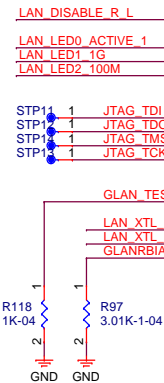
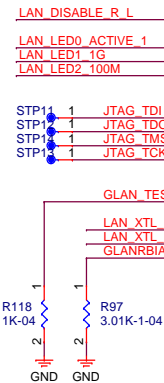
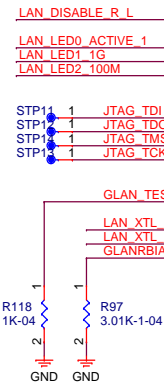
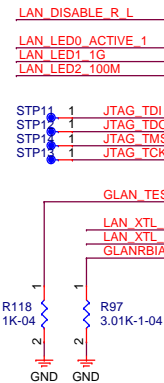
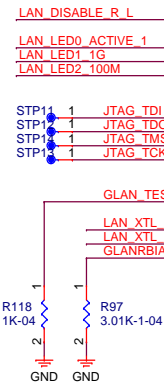
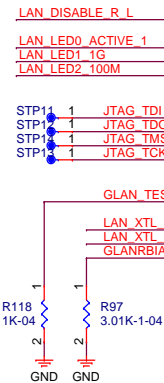
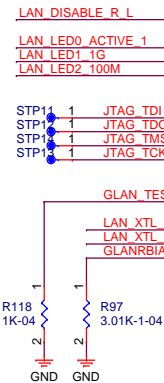
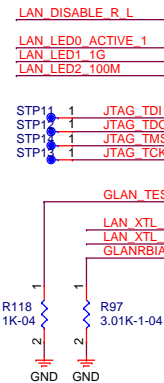
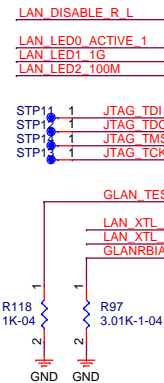
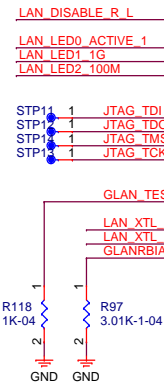
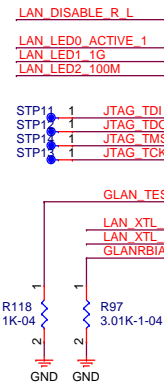
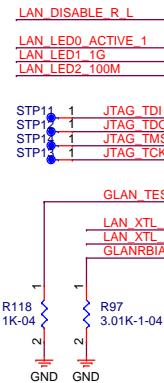
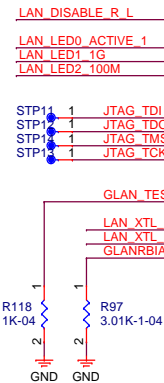
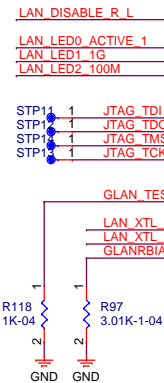
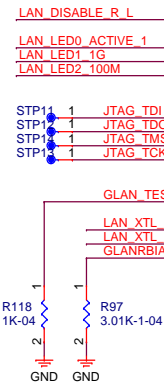
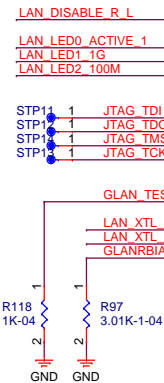
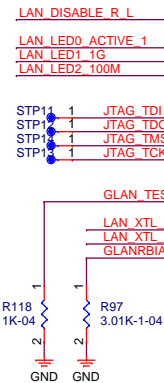
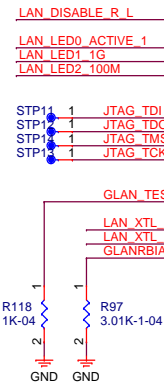
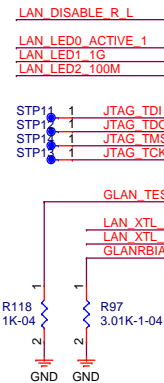
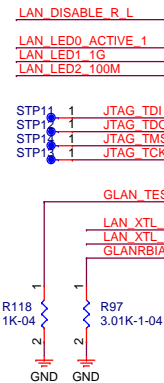
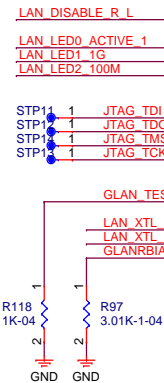
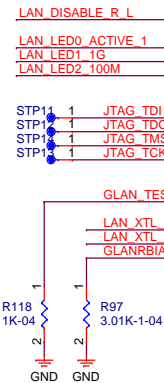
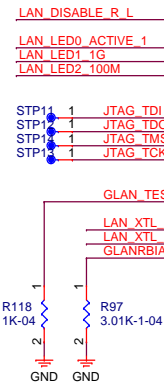
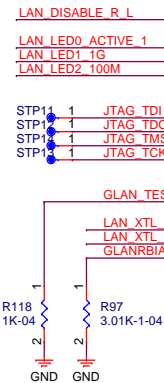
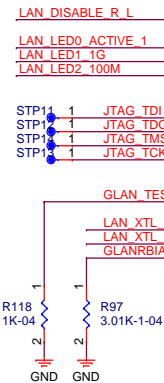
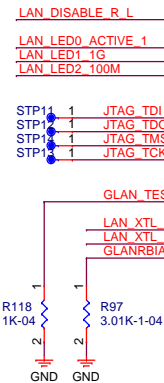
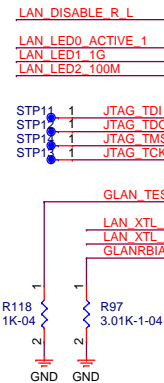
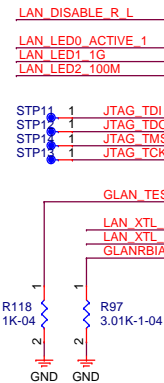
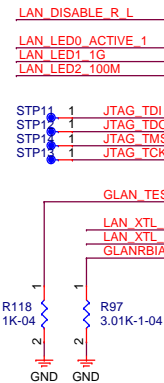
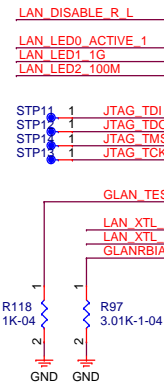
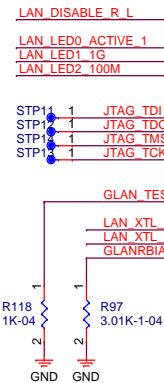
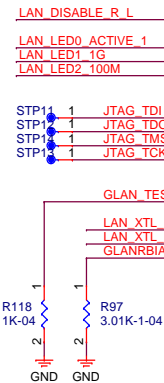
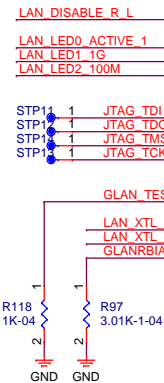
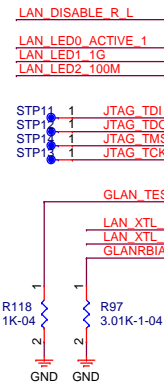
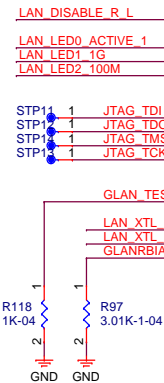
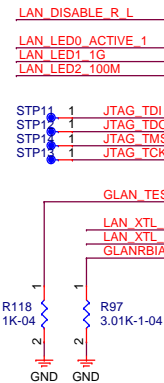
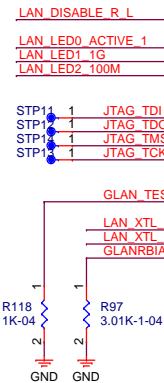
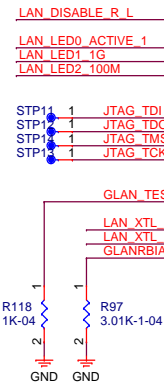
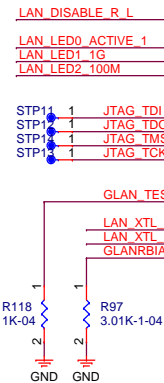
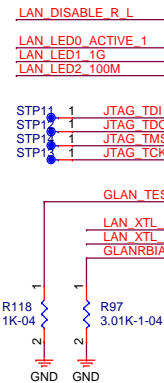
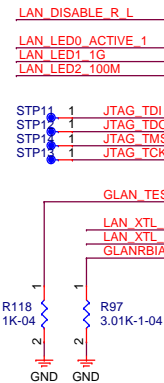
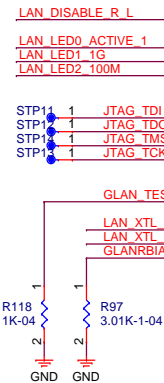
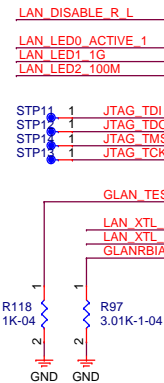
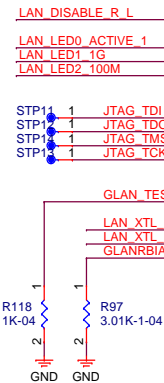
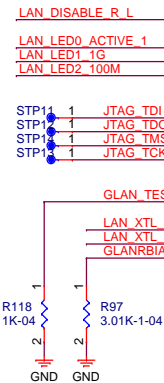
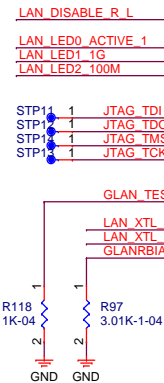
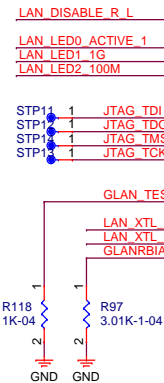
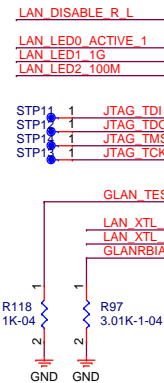
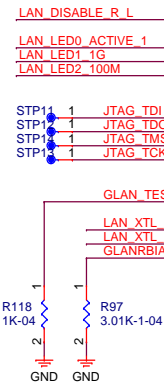
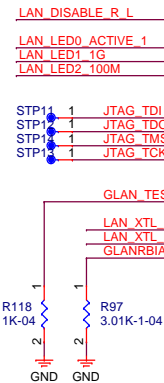
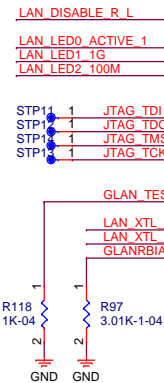
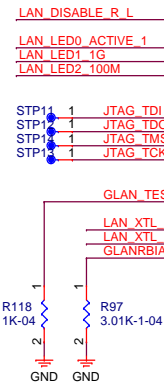
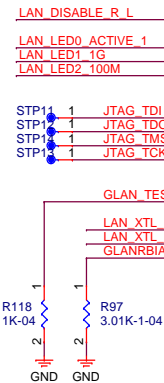
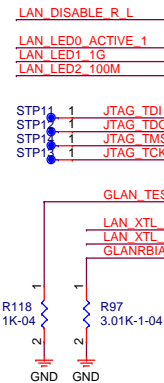
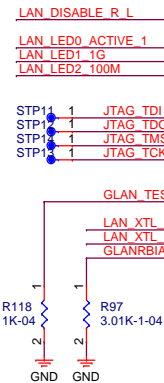
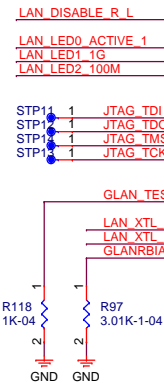
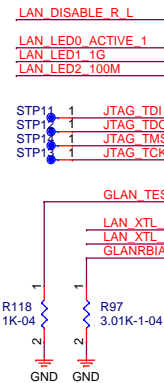
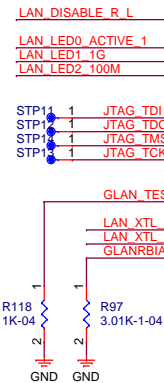
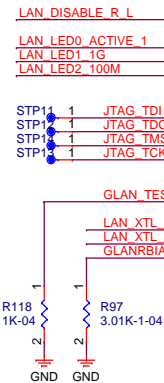
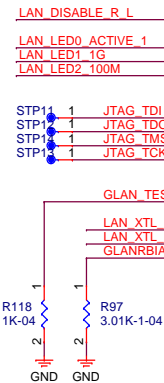
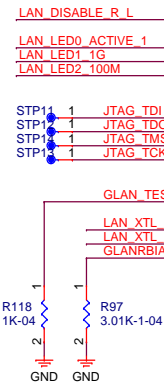
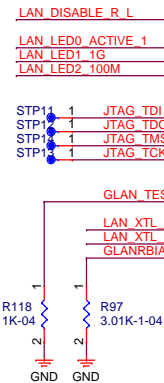
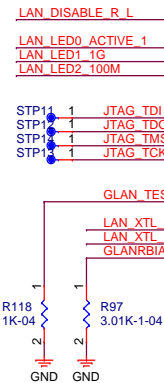
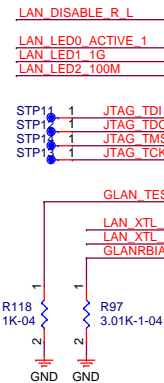
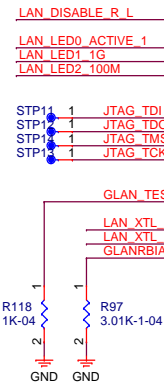
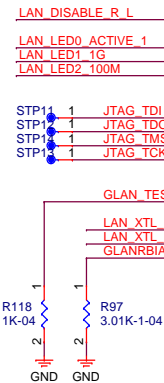
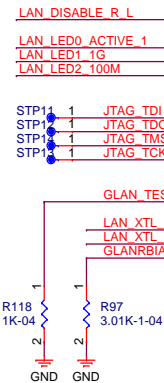
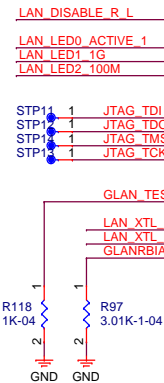
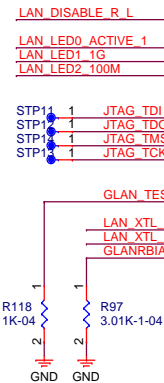
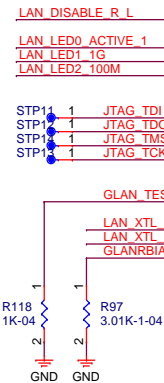
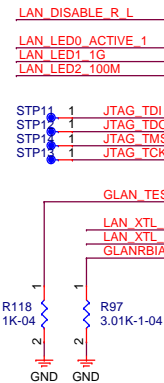
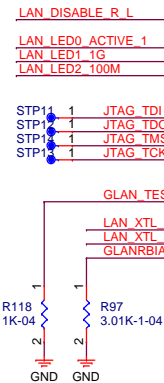
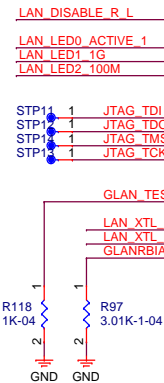
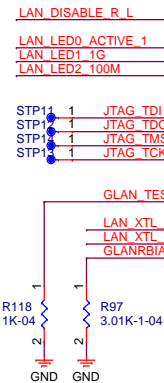
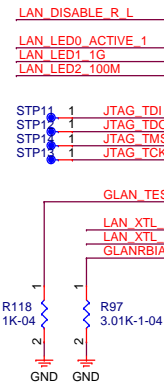
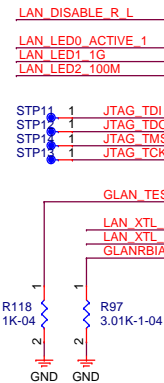
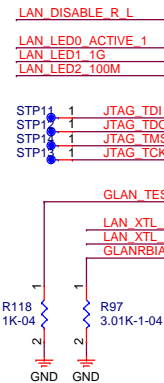
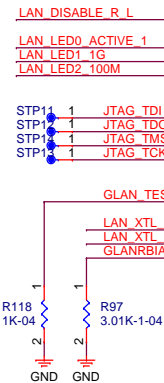
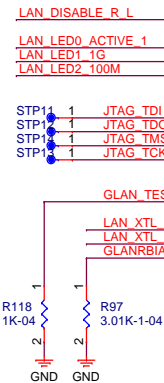
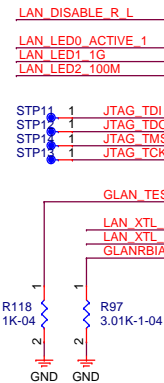
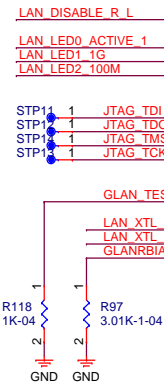
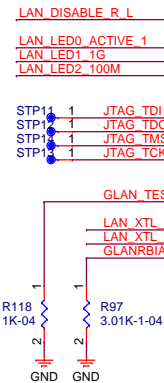
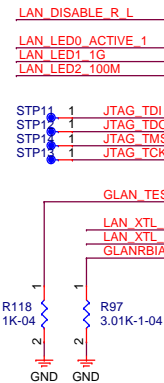
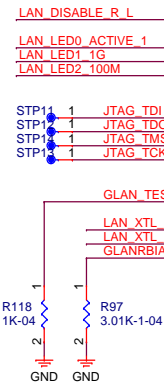
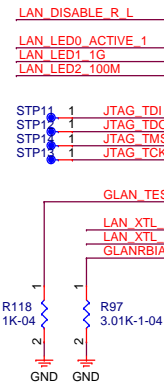
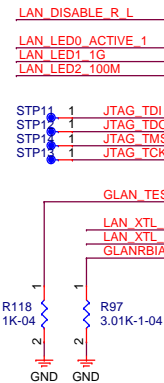
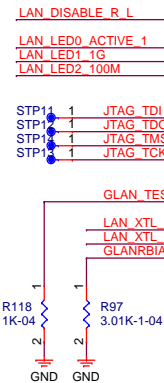
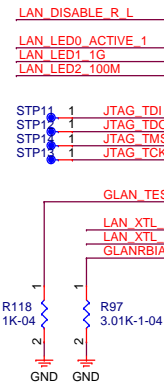
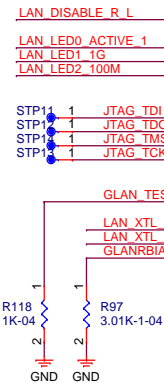
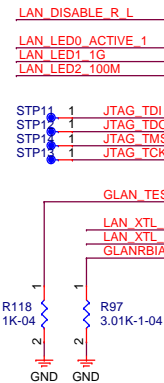
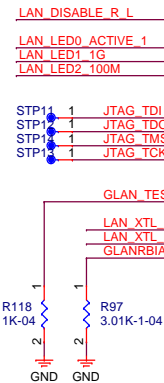
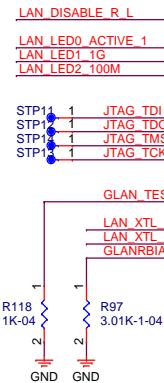
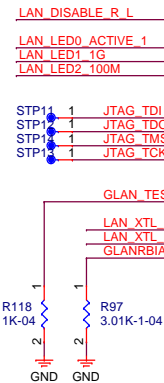
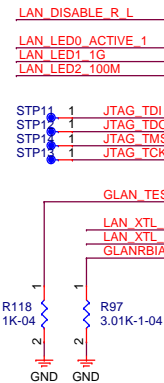
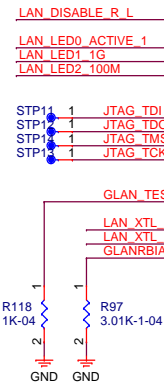
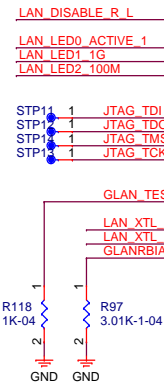
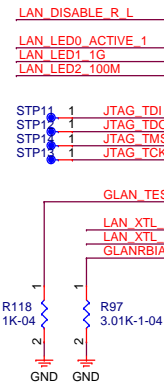
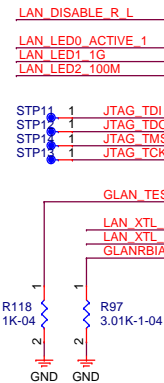
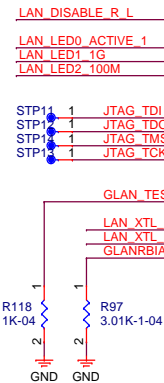
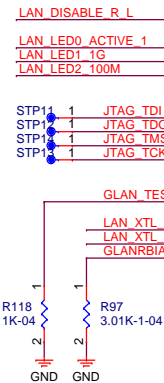
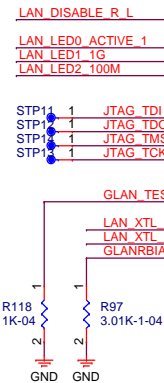
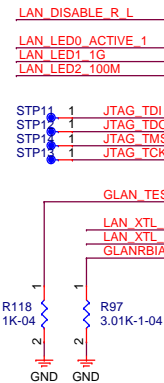
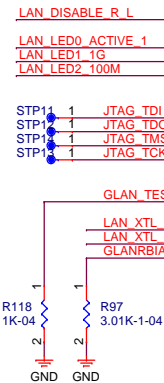
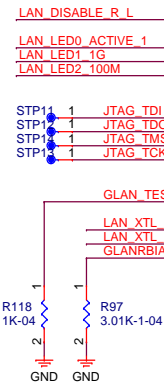
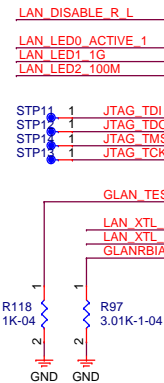
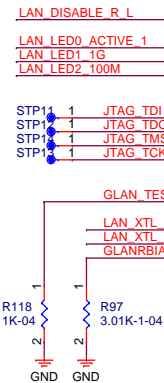
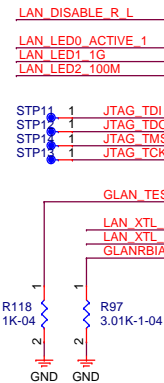
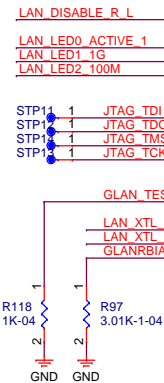
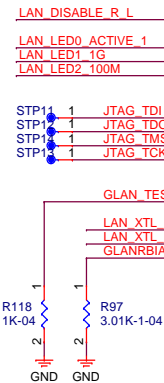
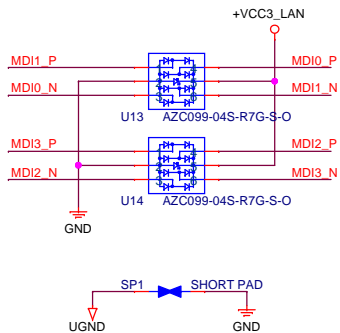
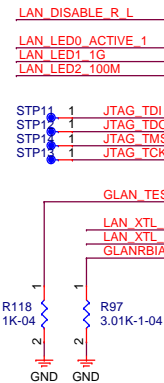
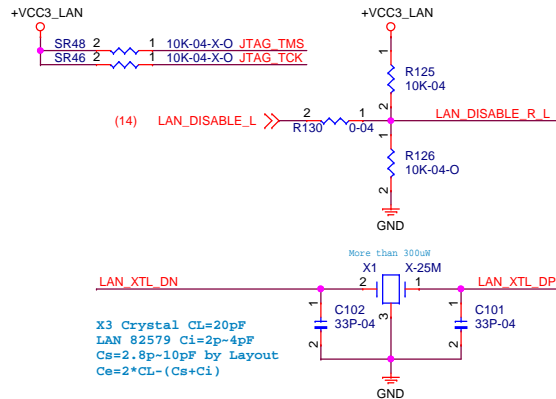
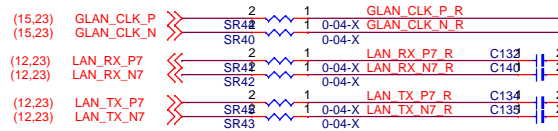
SMBUS Logic Circuit

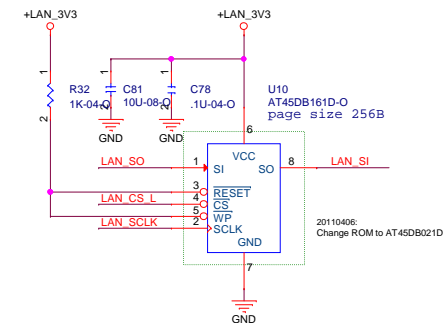
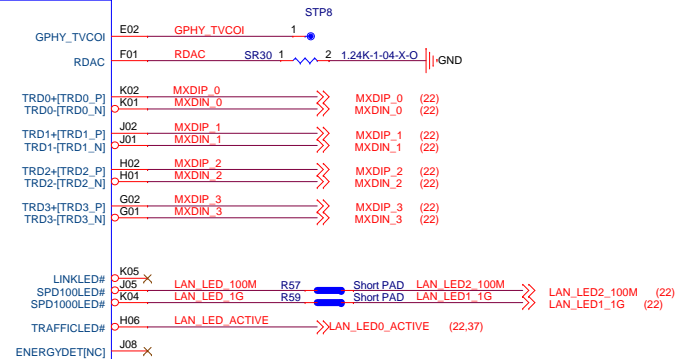
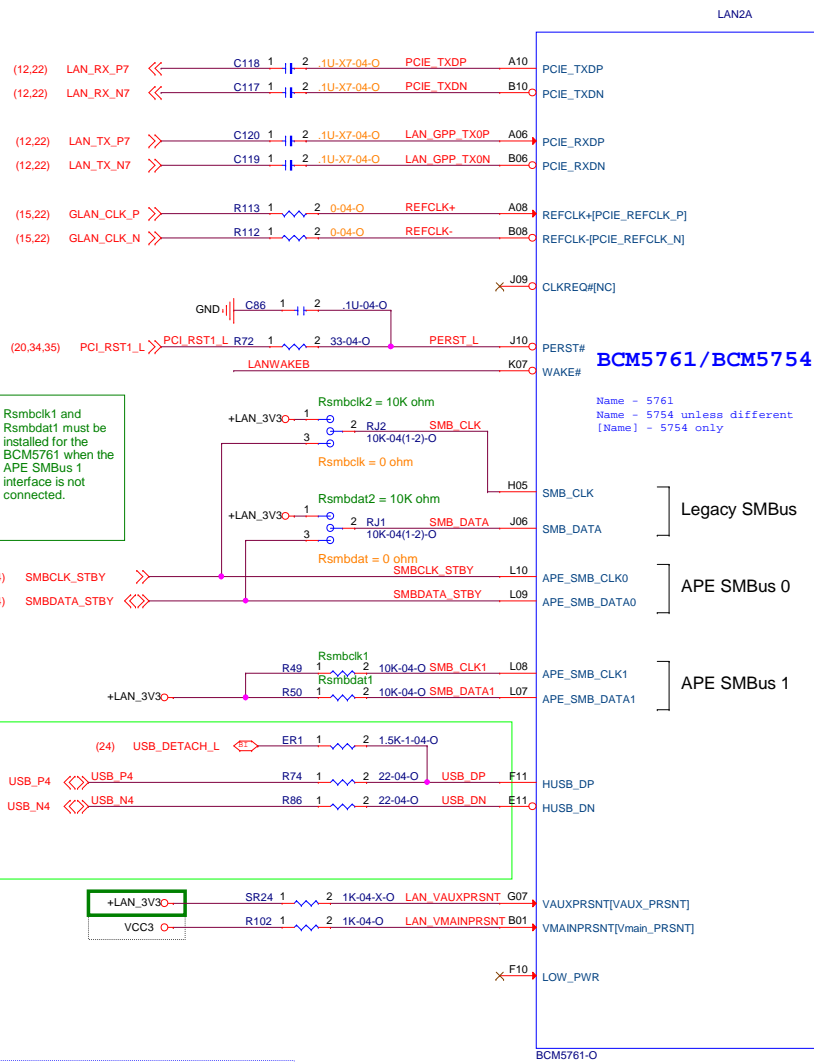


Layout Note:
SMBUS Trace Max 21500MILS



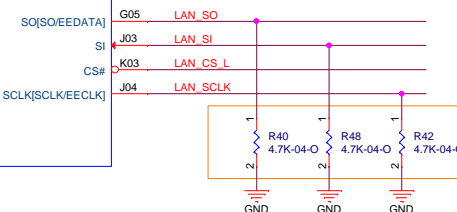
CRB V0.7 cHECK ok





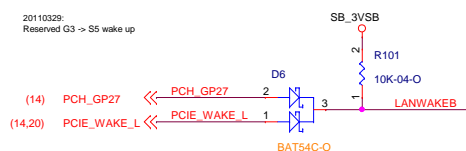
NV_STRAP1[NC] C10
NV_STRAP0[NC] D10

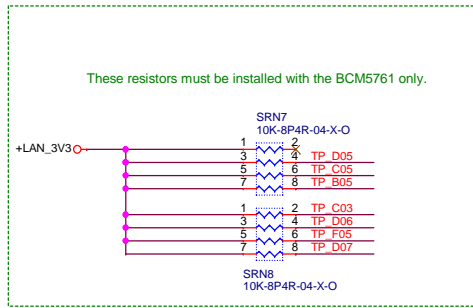
Flash device shown is for the BCM5761 only. Refer to the BCM5754 data sheet for supported flash devices.



These resistors must be installed with the BCM5754 to configure flash auto-sense.

20110329:
Reserved G3 -> S5 wake up

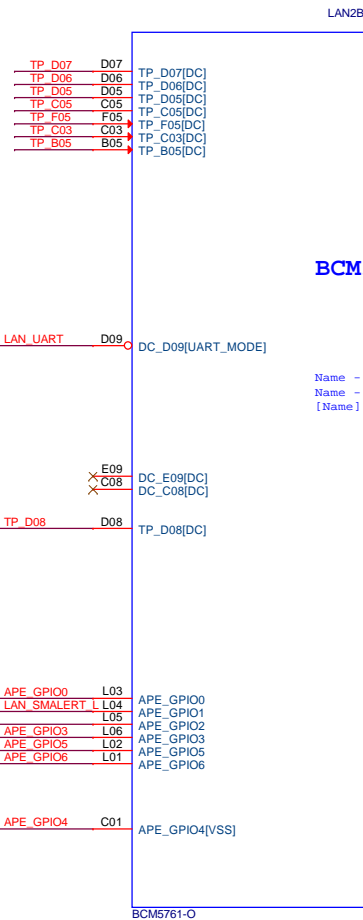




Ruart_mode should be installed to enable the debug UART function when the BCM5754 is used.

Rd8_pd must be installed with the BCM5761 only.

Rvss_5754 must be installed when the BCM5754 is used.



BCM5761/BCM5754

Name - 5761
Name - 5754 unless different
[Name] - 5754 only

GPIO1/SERIAL_D[GPIO_1/SERIAL_D]
GPIO2/SERIAL_D[GPIO2]
GPIO0[GPIO_0/SERIAL_D0]

E05 LAN_GPIO1 1 STP9
J07 LAN_GPIO2 1 STP5
D02 LAN_GPIO0 1 STP10
Rsmalert#
1 2 LAN_SMALERT_L
SR38 0-04-X-O

Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.

NC_C04[DC] C04 NC_C04 SR37 1 2 10K-04-X-O +LAN_3V3
NC_L11 L11 NC_L11 1 STP1
NC_K11 K11 NC_K11 1 STP3
NC_J11 J11 NC_J11 1 TP6
NC_H11 H11 NC_H11 1 TP7

For Energy Detection function use only for 5761E use

NC_K10[REFCLK_SEL] K10 NC_K10 R68 4.7K-04-O 1 2
D11 NC_D11 1 TP9
B03 NC_B03 1 TP10
Refclkssel
GND

Refclkssel must not be installed with the BCM5761, but may be installed with the BCM5754

TMS G10 TMS 1 TP8
TDO F08 TDO 1 TP1
TDI H07 TDI 1 STP7
TCK K09 TCK 1 STP6
TRST# K09 TRST_L 1 STP4

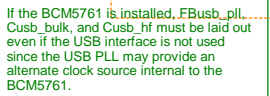
XTALO A04 LAN_XTALO 2 1 X-25M1
R114 200-1-04-O
C128 27P-04-O
GND
XTALI B04 LAN_XTALI
C127 27P-04-O
GND

Elitegroup Computer Systems

Title: **LAN (BCM5761) XTAL,GPIO**

Size: Custom Document Number: **Q77H2-AD** Rev: A

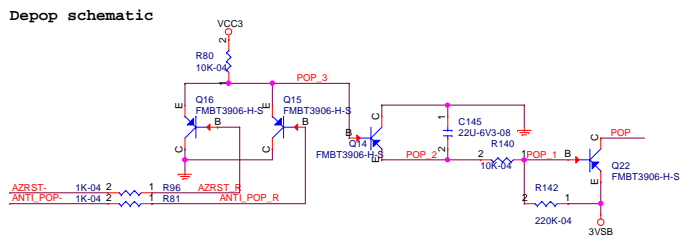
Date: Monday, October 31, 2011 Sheet 24 of 49



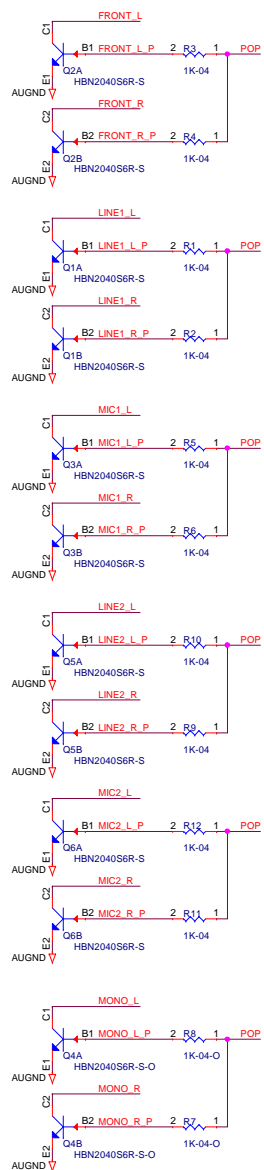
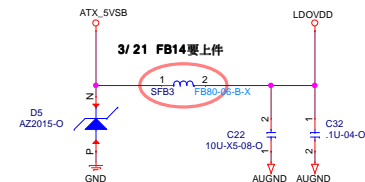
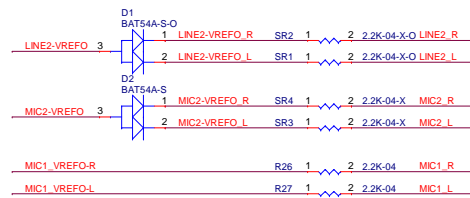
Qpnp25 and Cpnp25 must be installed with the BCM5754 only

The PWR_DWN[VDDP] ball must not be driven to 3.3V. Refer to the BCM5761 data sheet for logic thresholds and maximum ratings.

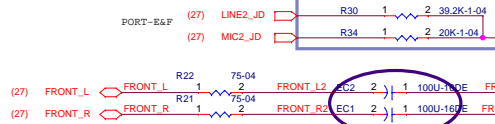
Depop schematic



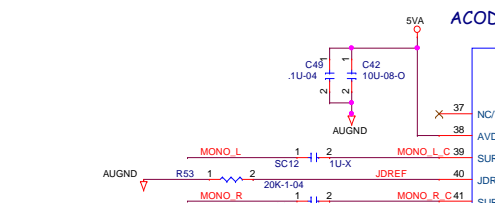
MIC Bias



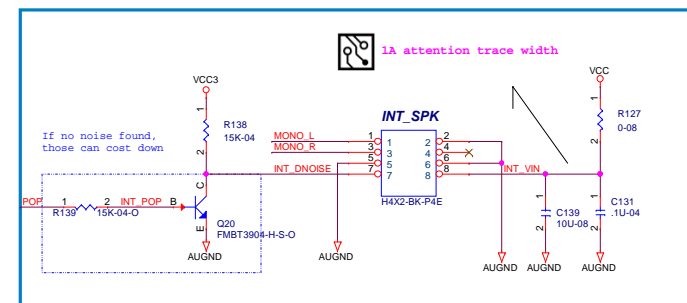
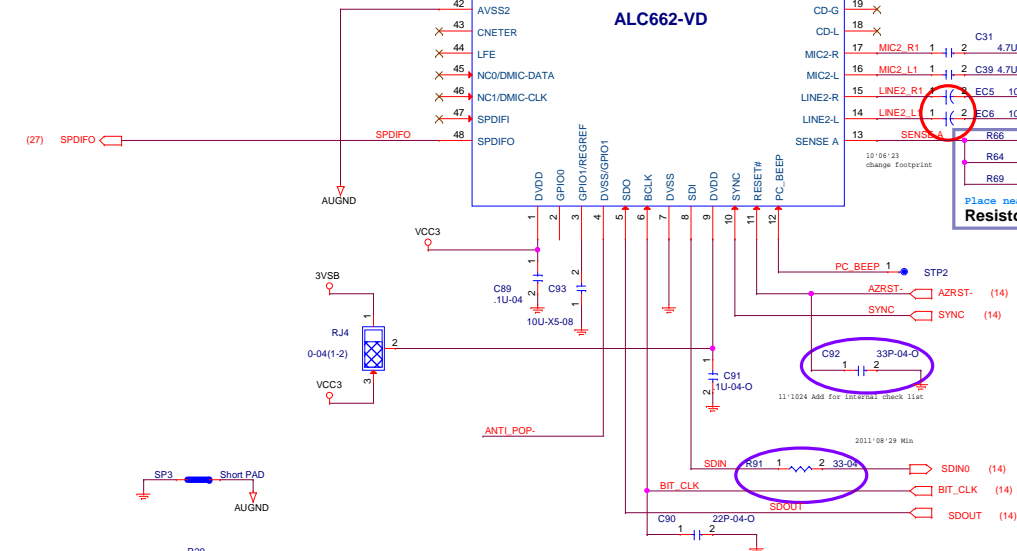
Resistors Networks



ACODEC1

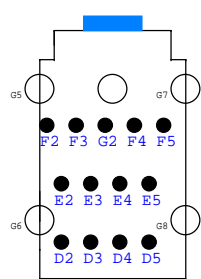
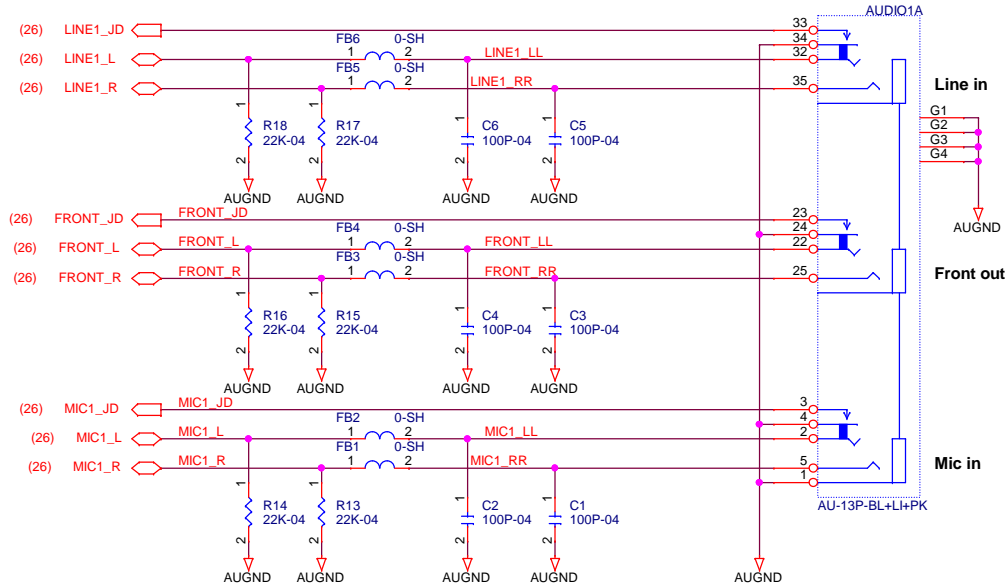


ALC662-VD

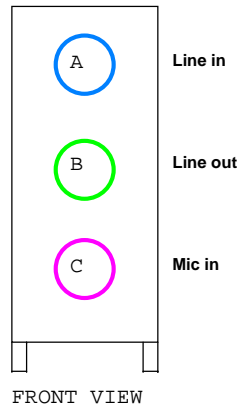


"INTERNAL SPEAKER"
FOR COMMERCIAL AND AIO SERIES USE

REAR-AUDIO

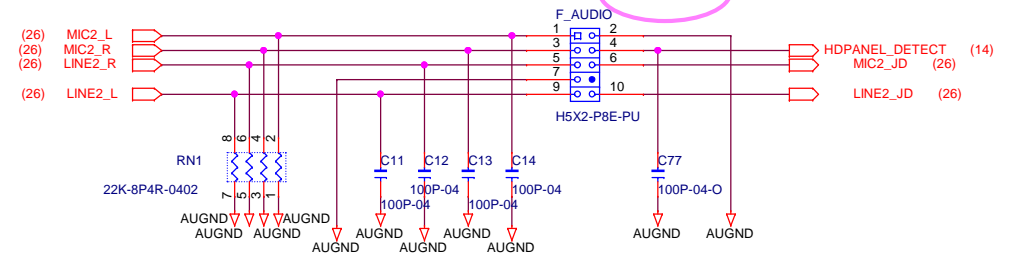


TOP VIEW

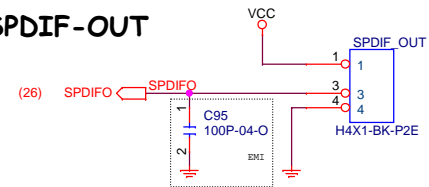


FRONT VIEW

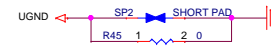
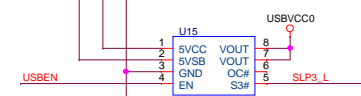
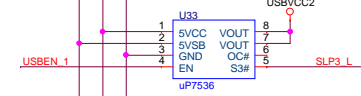
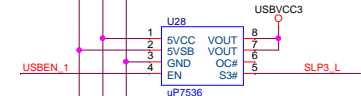
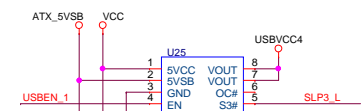
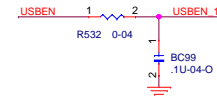
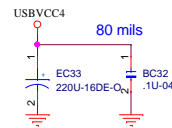
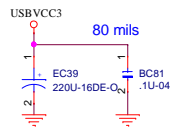
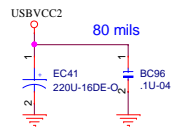
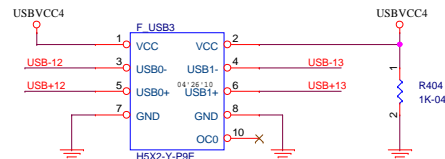
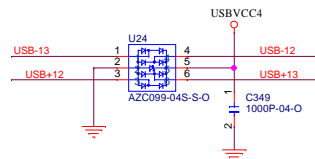
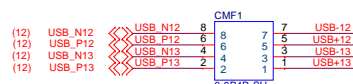
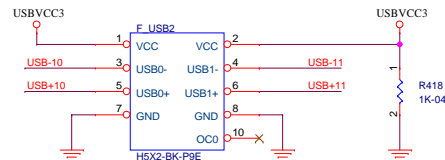
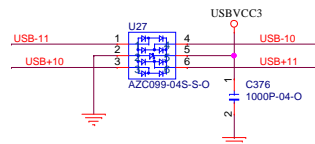
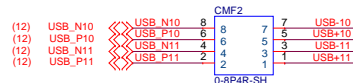
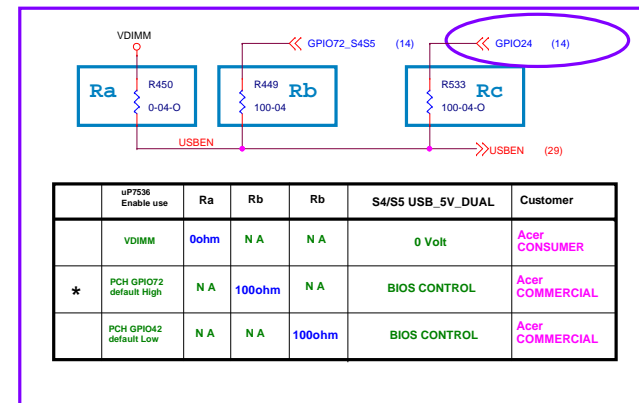
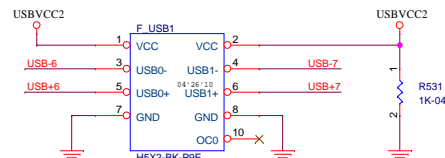
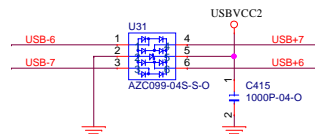
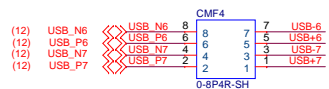
FRONT-AUDIO



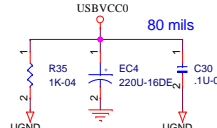
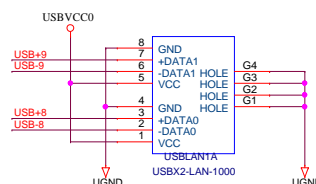
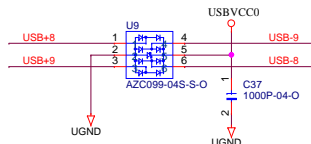
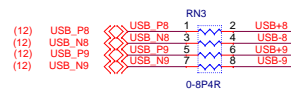
SPDIF-OUT

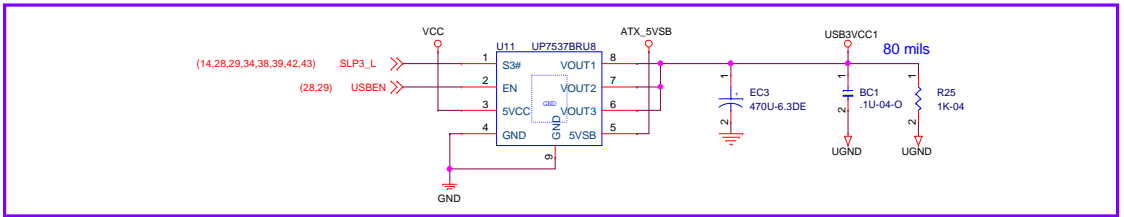
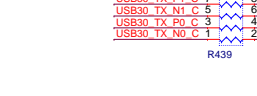
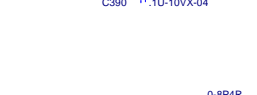
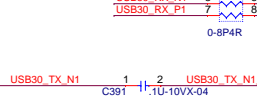
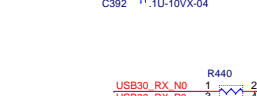
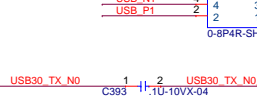
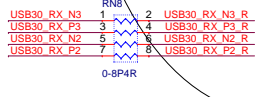
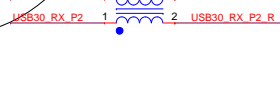
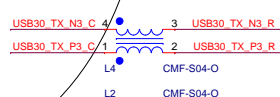
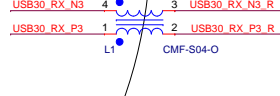
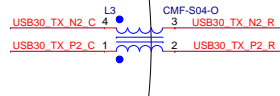
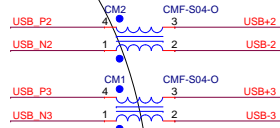
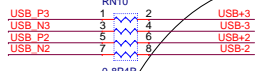


Title			
AUDIO ALC662 Connector (PANEL)			
Size	Document Number	Rev	
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Date:	Monday, October 31, 2011	Sheet	27 of 49

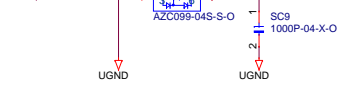
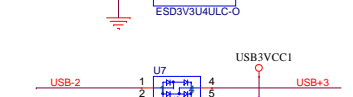
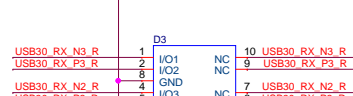
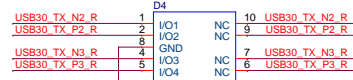


FRONT PANEL USB2.0 HEADER REAR PANEL USB2.0 CONNECTOR

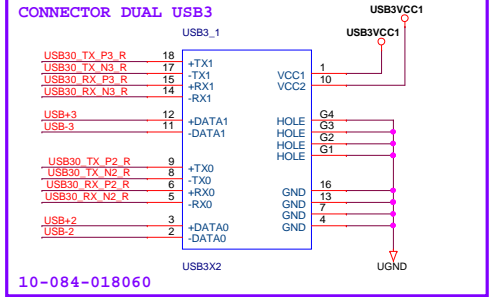




USB3 ESD COMPONENTS

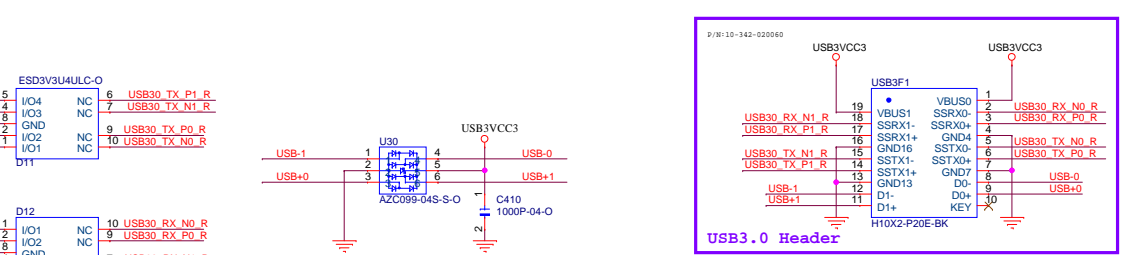
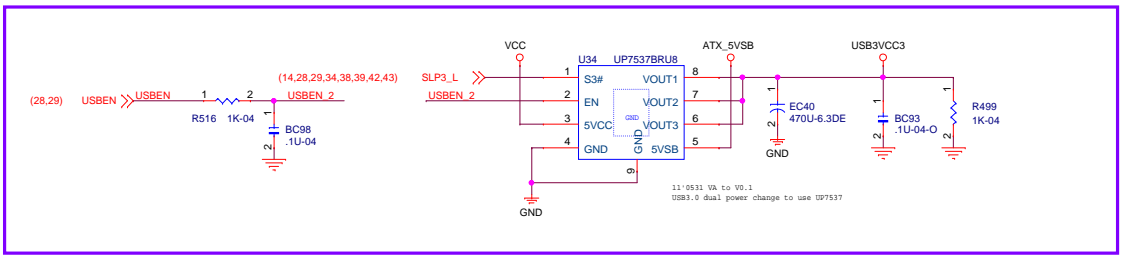


NOTE: Port1,Port2 SWAP between Port3, Port4
2011'03'11



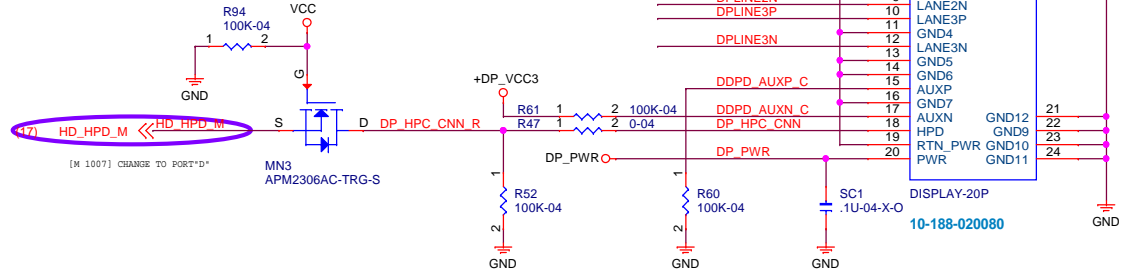
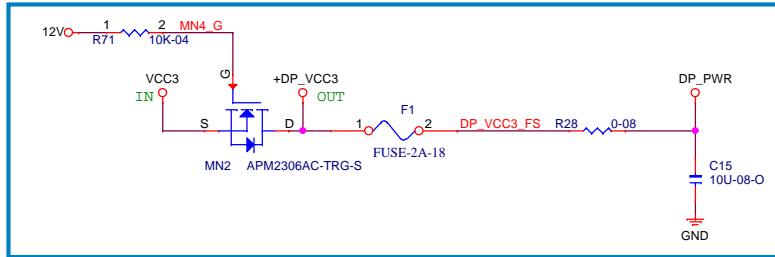
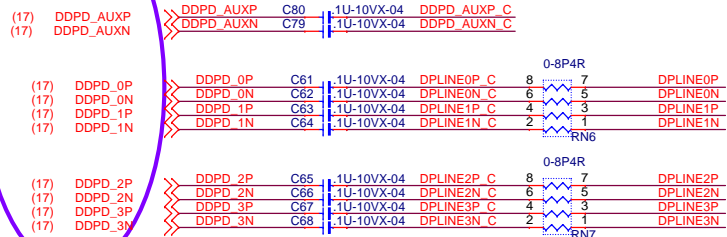
REAR PANEL USB3.0 CONNECTOR

FRONT PANEL USB3.0 HEADER



USB3 ESD COMPONENTS

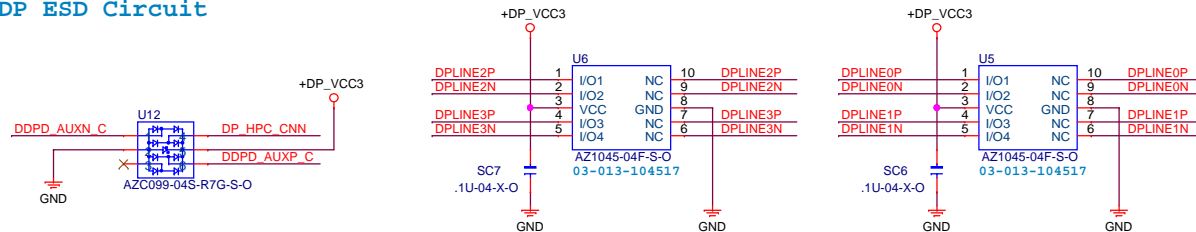
[M 1007] CHANGE TO PORT"D"



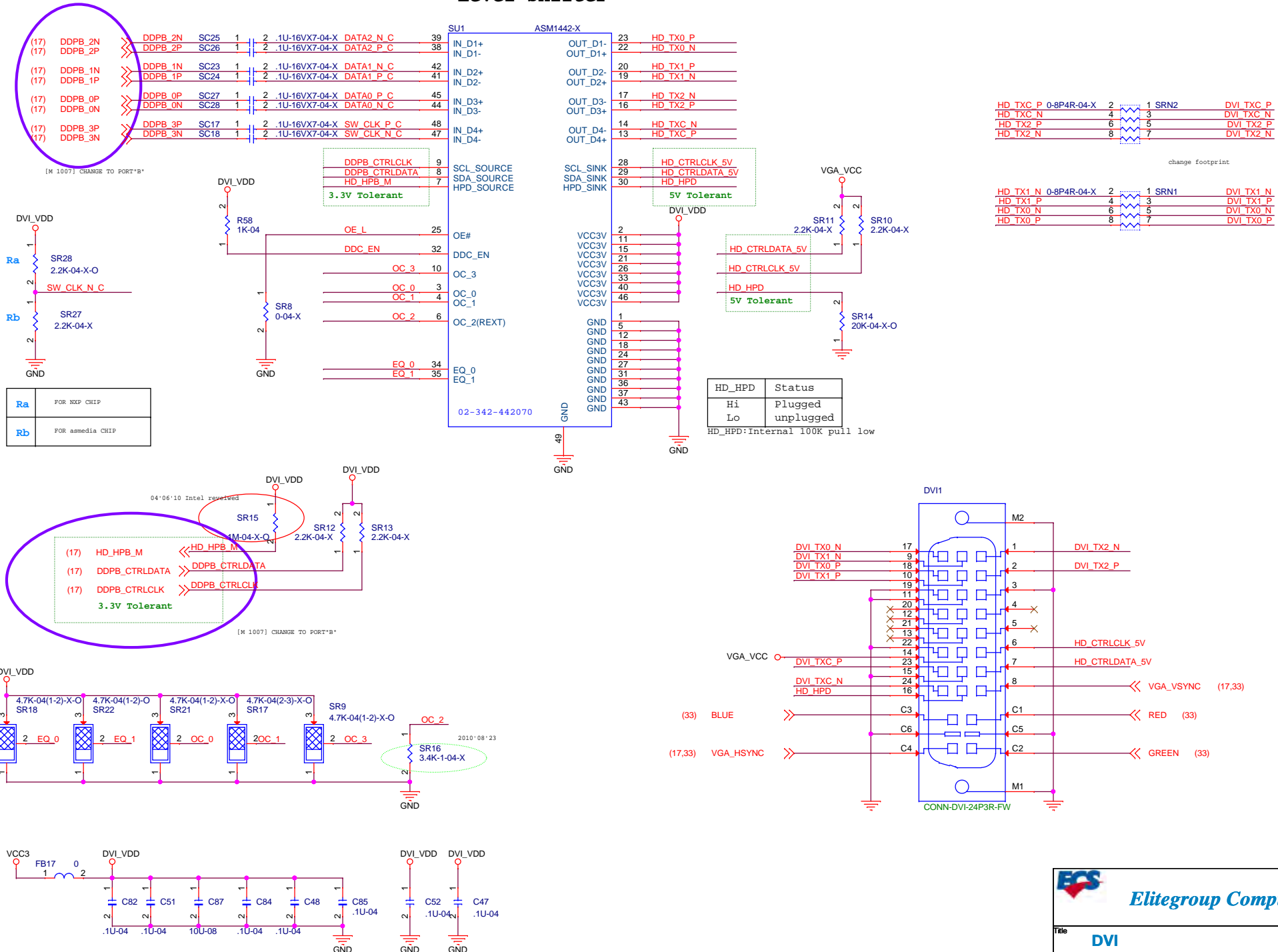
2011/10/17 [Min] DEL DP Port2 support HDMI DONGLE

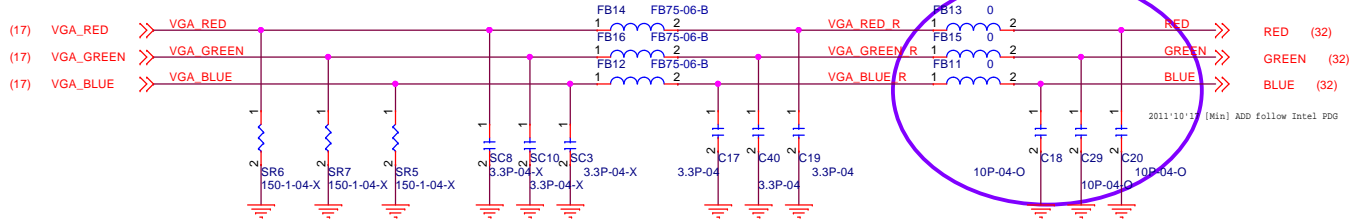
SUPPORT DP TO HDMI/DVI DONGLE

DP ESD Circuit

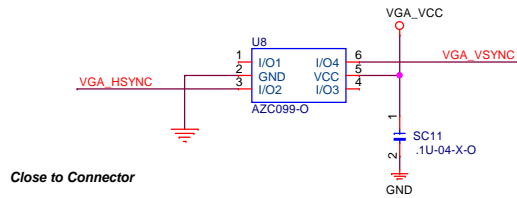
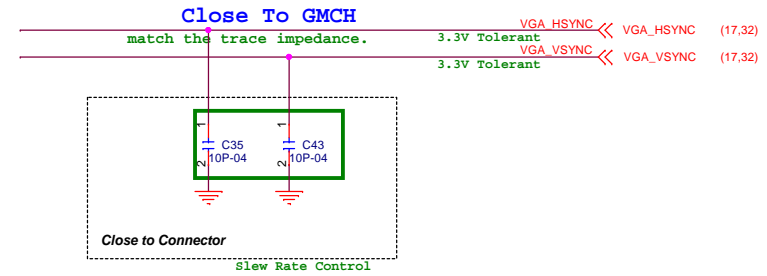


Level Shifter

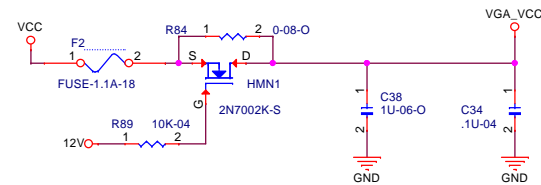




Close to Connector

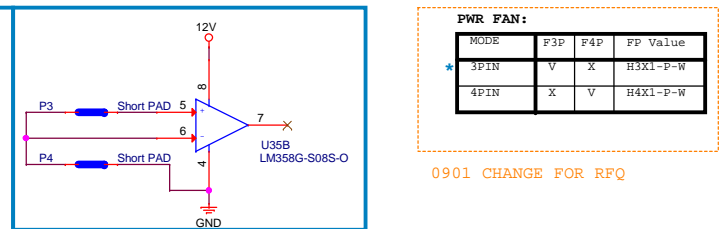
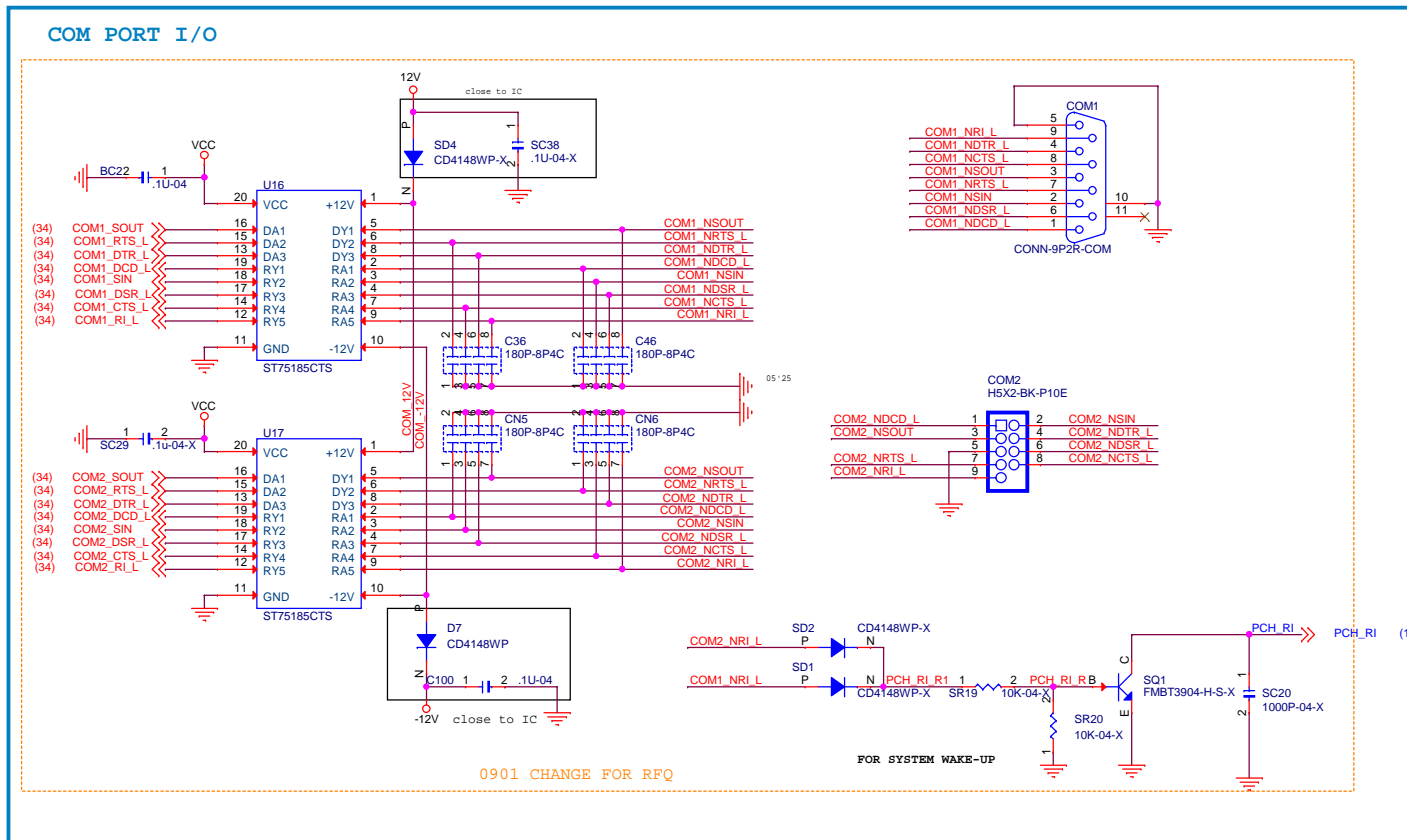
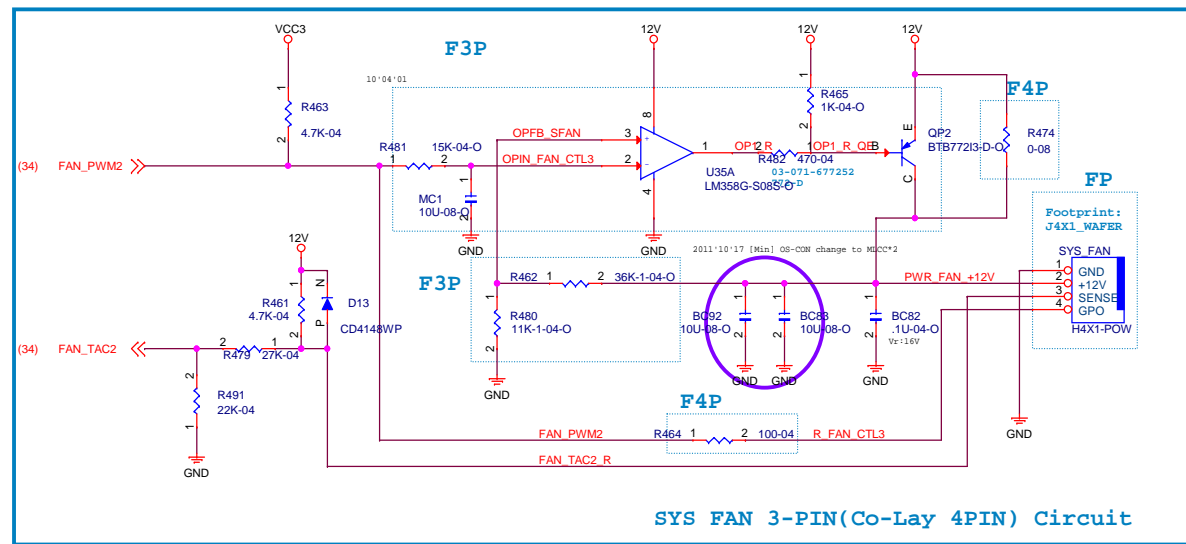
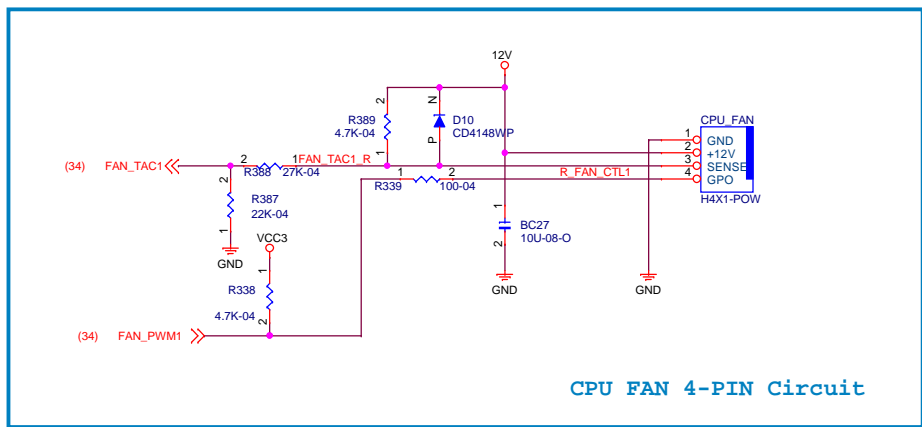


If build in Internal DVI/HDMI Con,
that can use the circuit to protect reverse voltage together.

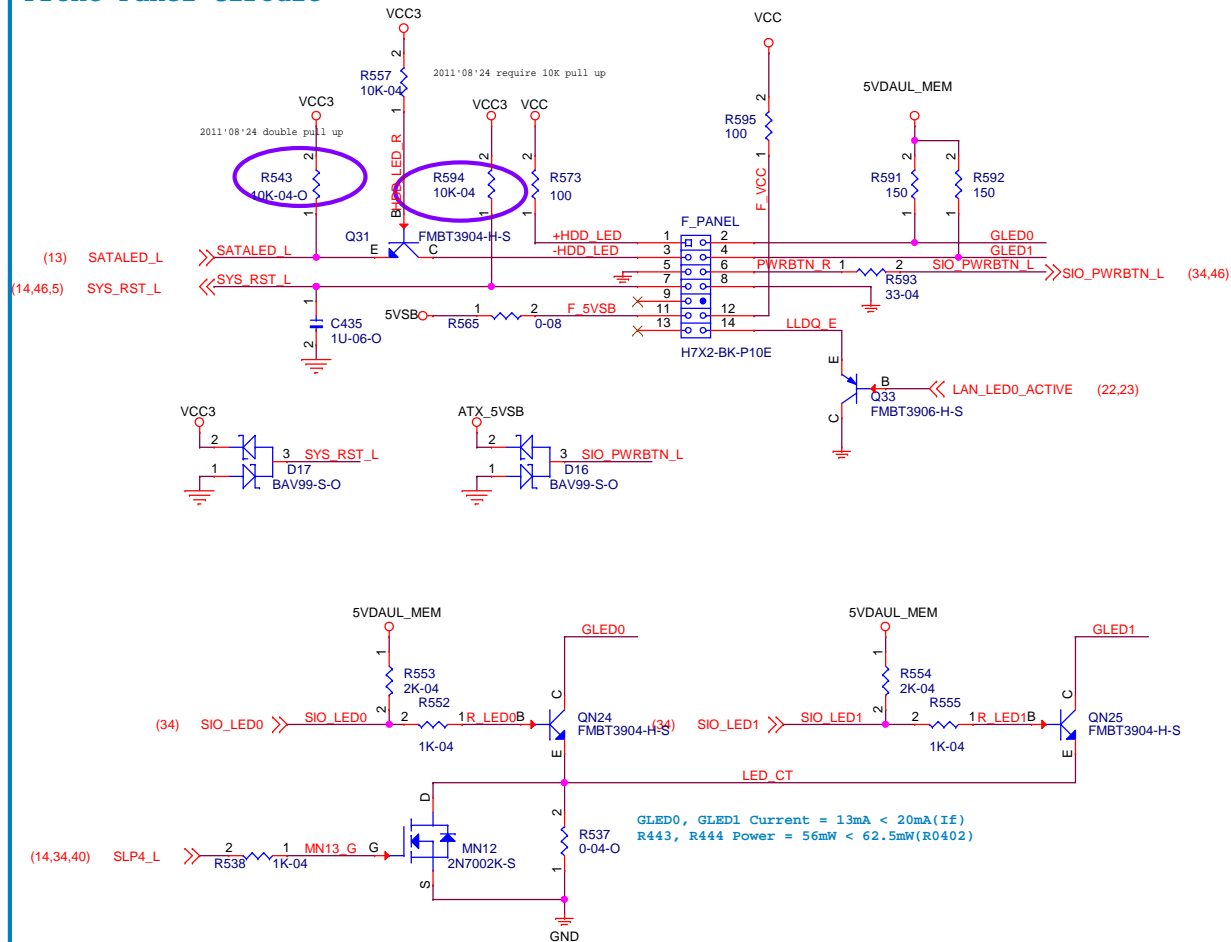


Close to Connector

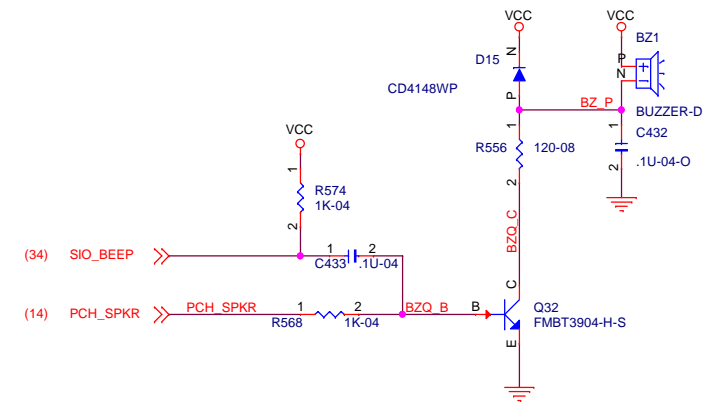




Front Panel Circuit

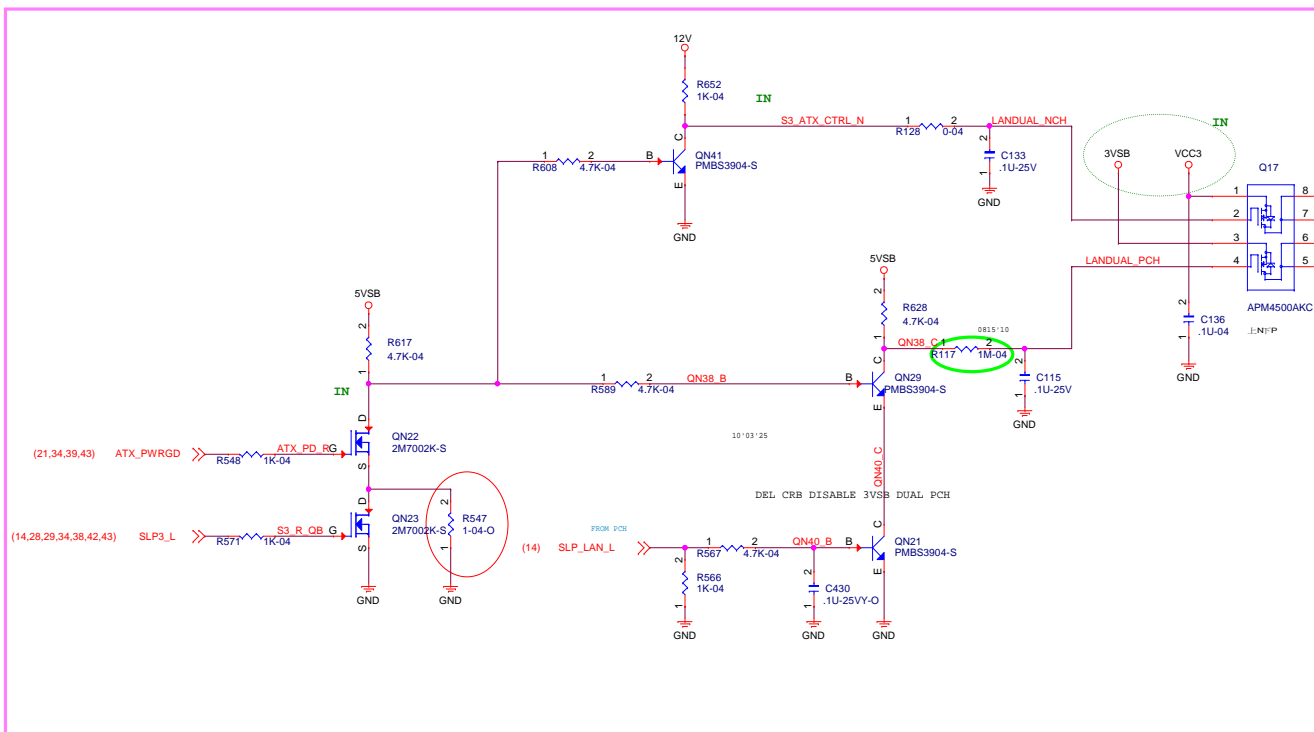


Buzzer Circuit

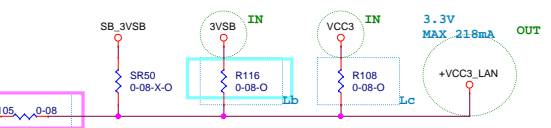


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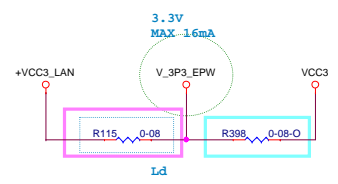
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F_PANEL, BUZ		
Size	Document Number	Rev
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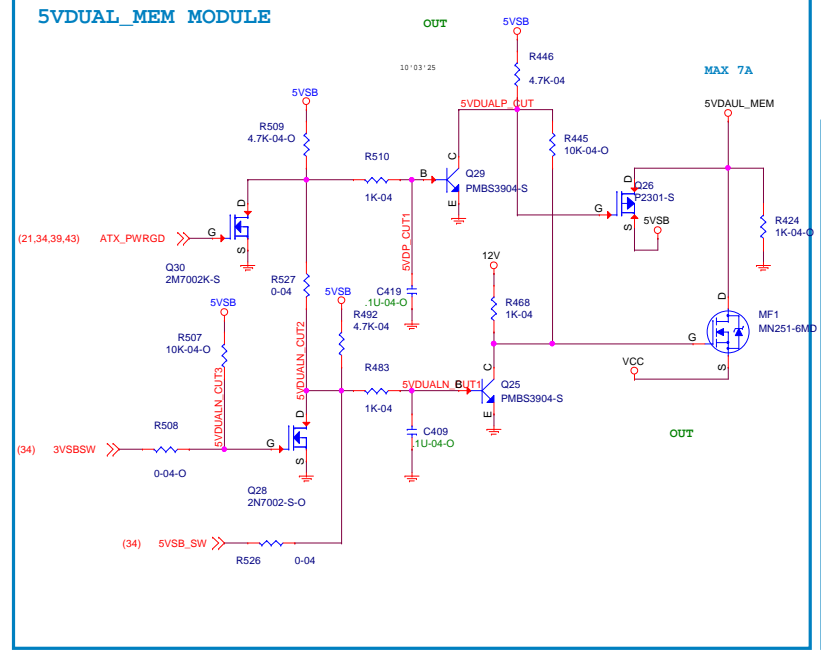
AMT 上件
NON AMT 上件



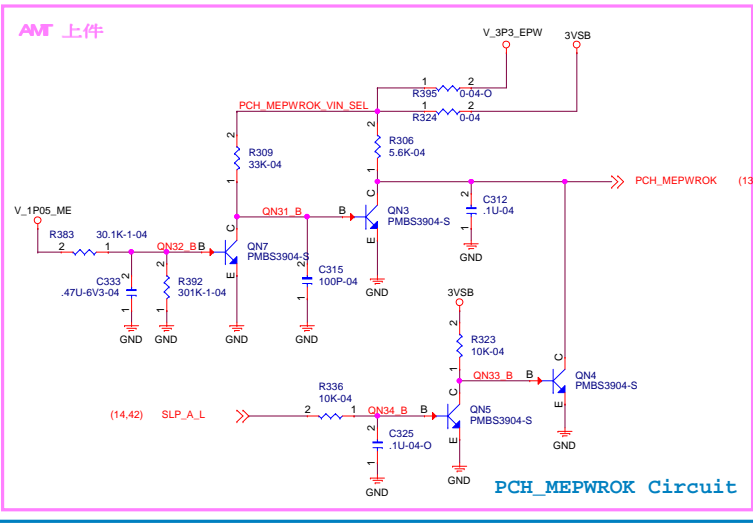
LAN Power Source	La	Lb	Lc
3V LANAUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN (NO WGL) or M0 Only	X	X	V



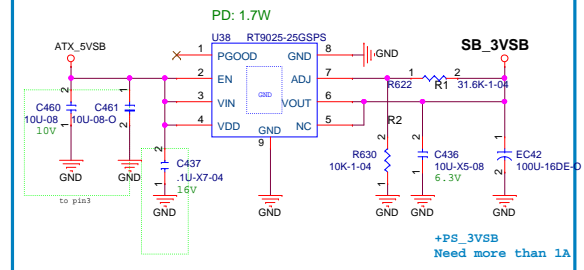
5VDUAL_MEM MODULE



AMT 上件



+3VSB Circuit





VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (\text{EQ. 1})$$

- I_{SS} is the soft-start current source at the 20 μ A limit
- V_{SRFF} is the buffered V_{RFF} reference voltage

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}
1	1	SW0	VSET1	VOUT1
1	0	SW1	VSET2	VOUT2
0	1	SW2	VSET3	VOUT3
0	0	SW3	VSET4	VOUT4

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (\text{EQ. 21})$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 22})$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{REF} + R_{SET2}} \right) \quad (\text{EQ. 23})$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

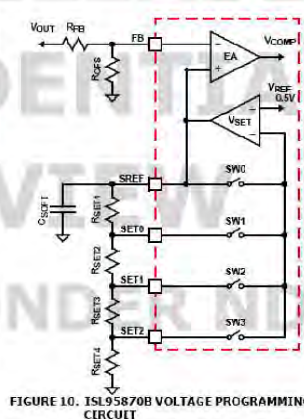
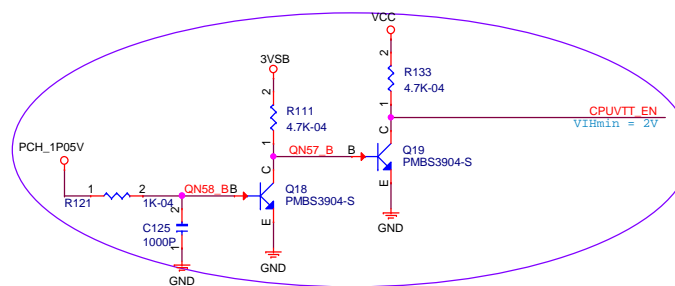
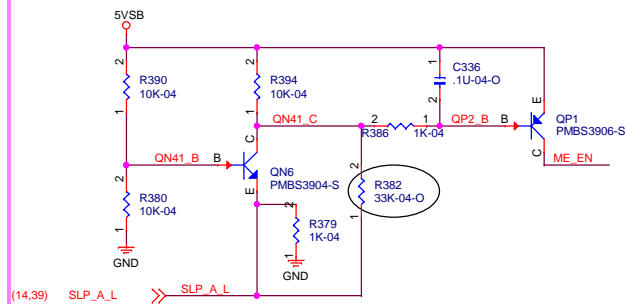
$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (\text{EQ. 24})$$


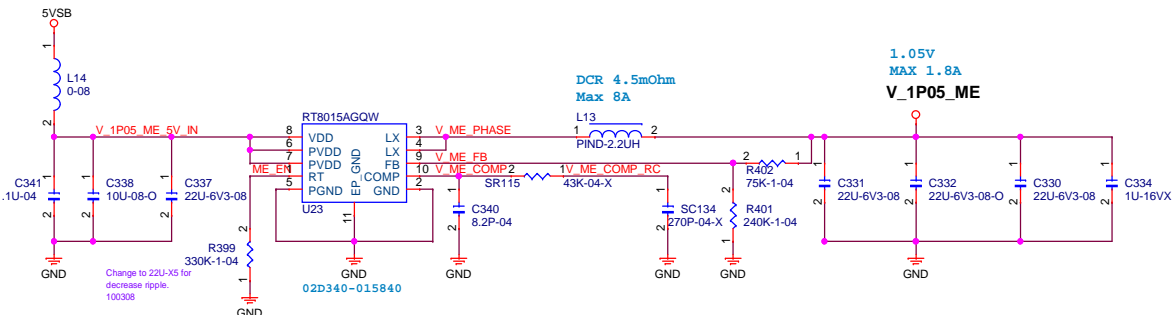
FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC





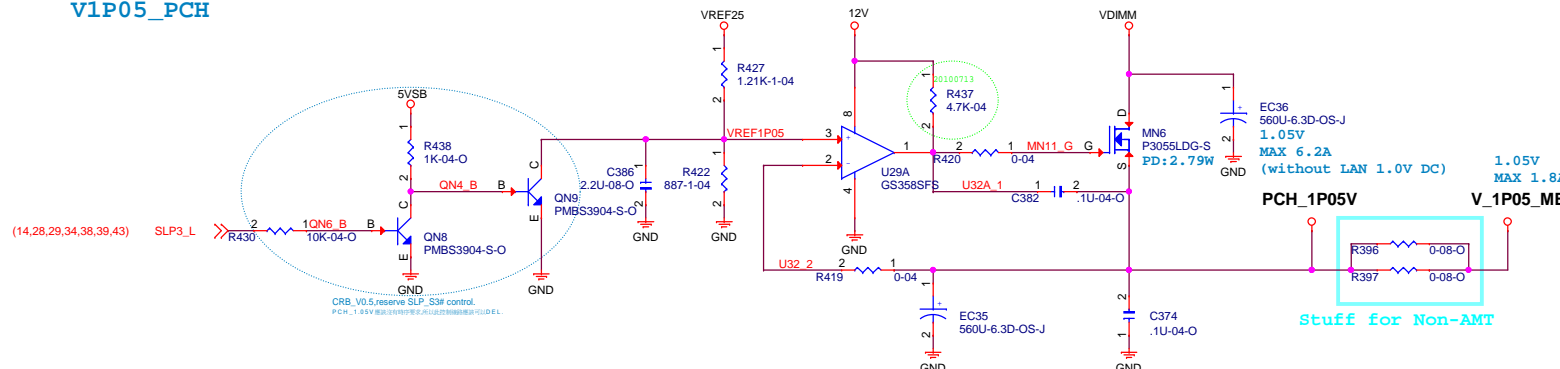
SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable



V1P05_ME

AMT 上件

V1P05_PCH



BOM Note:

02-340-015840...dnt10, n8106a
IC REG.RT8015AGQW.WDFN 10P.3A LEAD-FREE(RoHS/HF).
RICHTEK

06-413-225094...choke, 22m, p14d9x4d6mm
POWER IND 2.2uH 20% 8A 4.5m OHM DIP-2P 8.2*8.2*7.5*6.7
mm AKL0806MN-2R2W-L3.2...LEAD-FREE(RoHS/HF).MAGIC

05-152-750113
RES.75K, 1/16W, 1%, SMD 0402...LEAD-FREE(RoHS/HF).

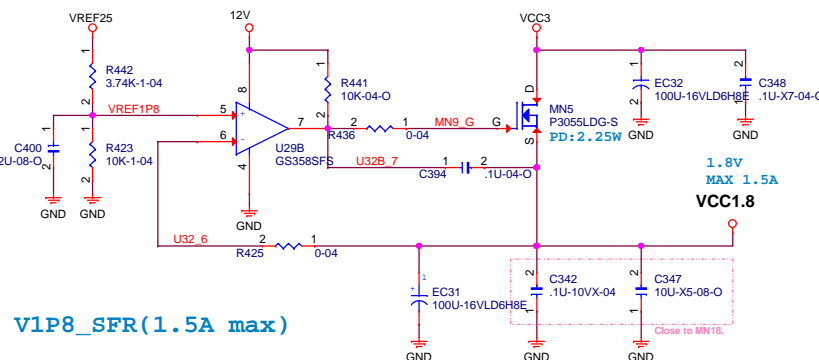
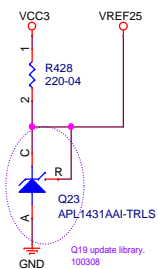
05-152-430103
RES.43K, 1/16W, 5%, SMD 0402...LEAD-FREE(RoHS/HF).

05-152-240114
RES.240K, 1/16W, 1%, SMD 0402...LEAD-FREE(RoHS/HF).

04-890-829100
C/C 8.2pF, 50V, 0.25pF...SMD 0402...LEAD-FREE(RoHS/HF).

Stuff for Non-AMT

VREF25



V1P8_SFR(1.5A max)

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Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*

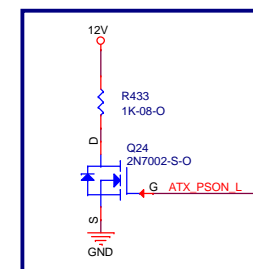
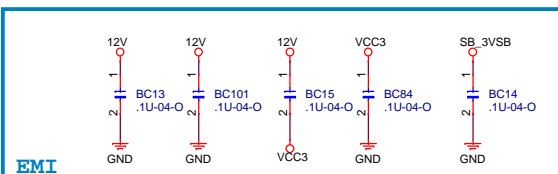
VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

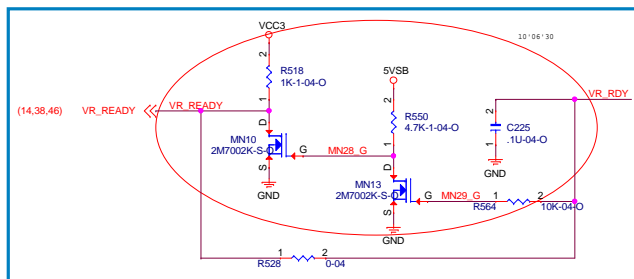
OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



(38) VR_EN
(5) VR_SVID_ALERT_L
(5) VR_SVID_DATAOUT
(5) VR_SVID_CK
(5) VR_HOT_L

(5) VCC_SEN
(5) VSS_SEN

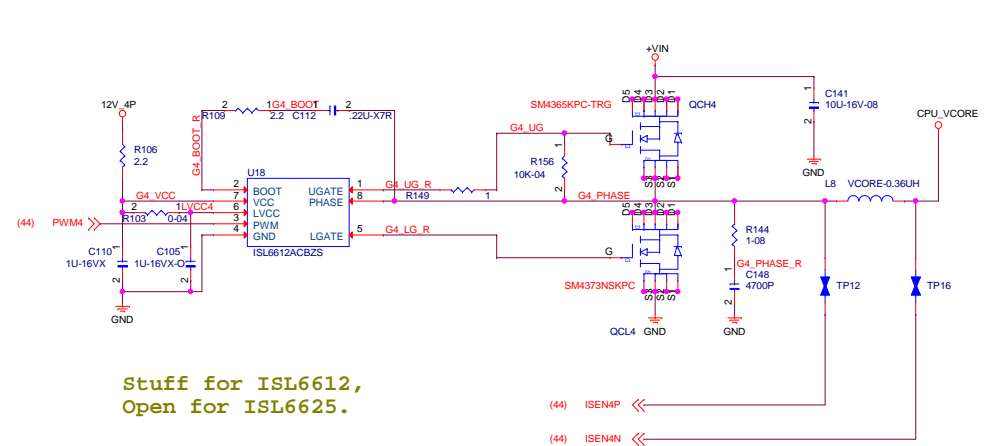
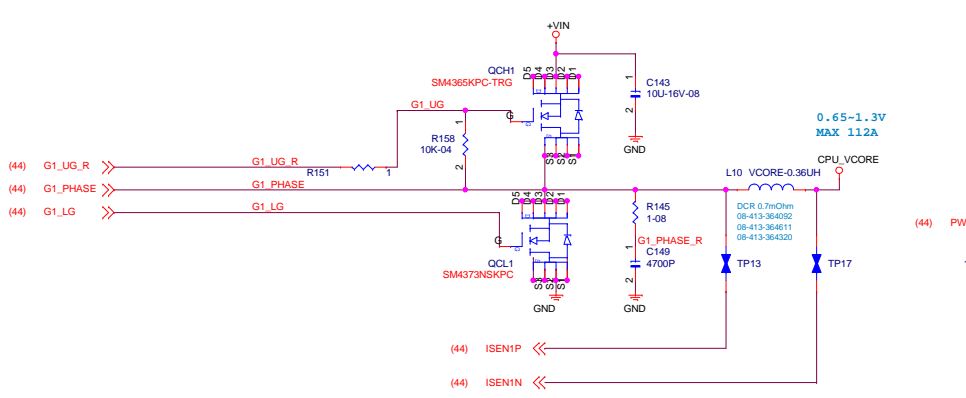
(5) VCCAXG_SEN
(5) VSSAXG_SEN



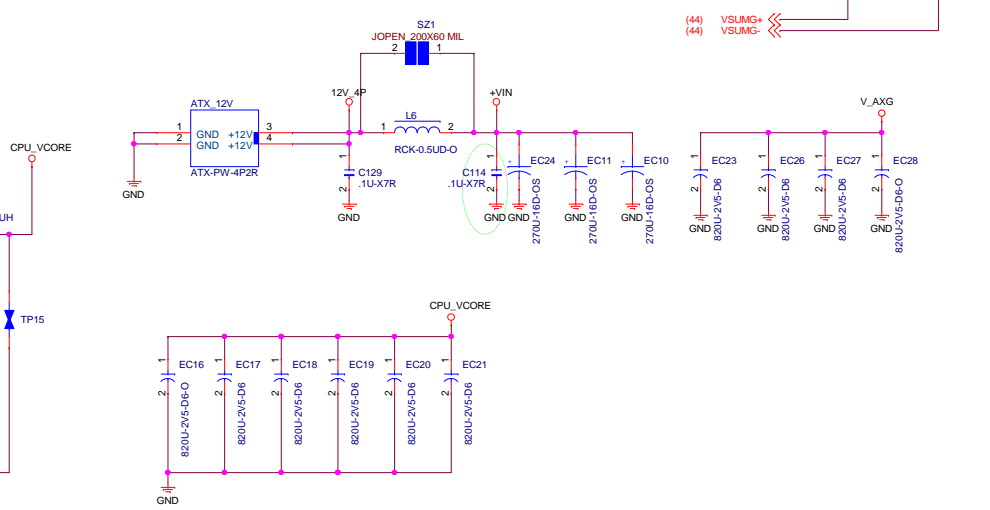
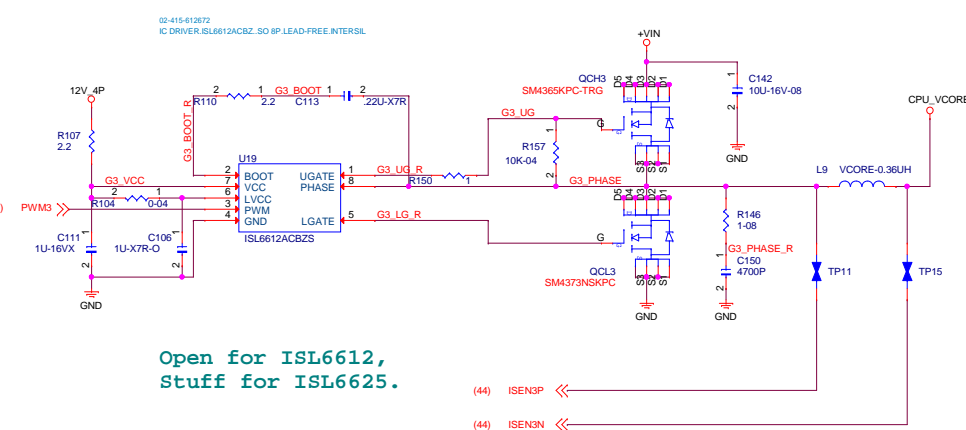
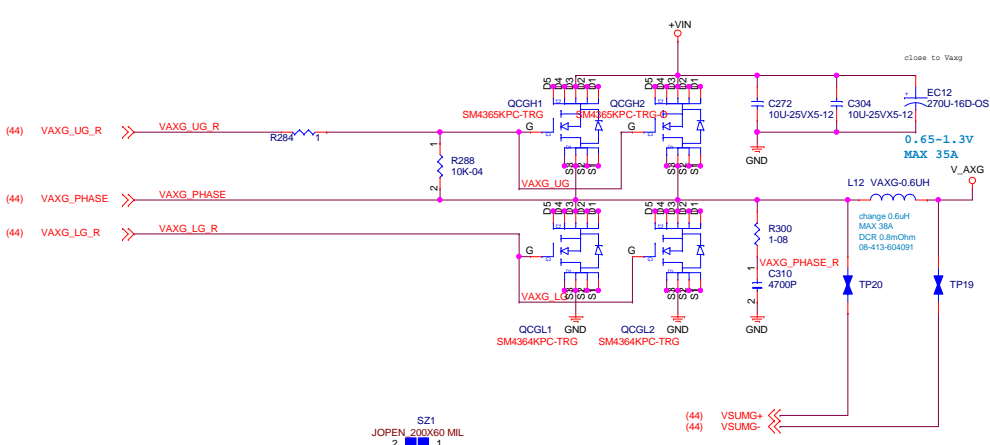
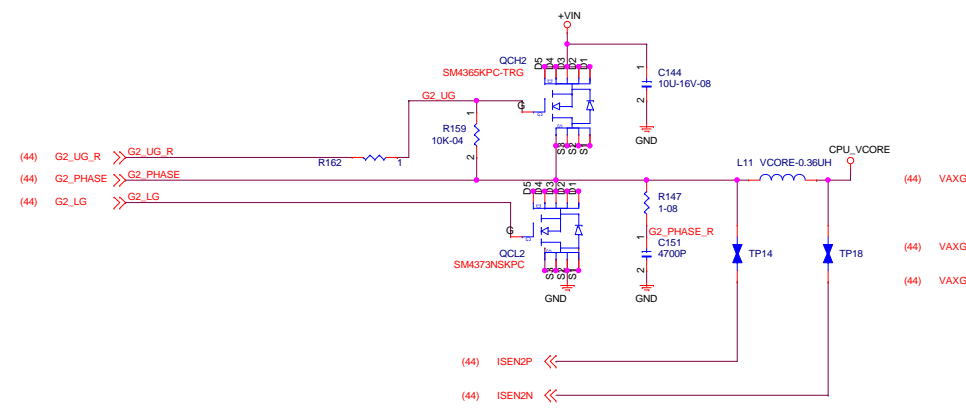
For VR_READY Power On Sequence

Elitegroup Computer Systems

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Stuff for ISL6612,
Open for ISL6625.



Open for ISL6612,
Stuff for ISL6625.

